FABRICATION and CHARACTERIZATION of LOW-NOISE CRYOGENIC Si JFETs

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We have custom made Si JFETs with the intent of realizing good low-frequency noise at temperatures in the liquid-nitrogen and liquid-argon range—where the noise of commercial JFETs has typically risen to undesirable levels. We report initial results from the first fabrication lots and for measurements in several circuit configurations, yielding noise voltage levels as low as ≈10–20 nV/Hz$^{1/2}$ at 1 Hz for a 12 μm x 2500 μm gate JFET ($K_f \approx 10 \cdot \mu V^2 \cdot \mu m^2$).

There are a number of situations where it is useful to operate a low-noise transistor in a cryogenic environment. For applications that demand the lowest possible noise at low frequencies (≤10 kHz) where "1/f" noise is usually a problem, the device of choice is the Si JFET, even though its operation is limited to temperatures above ≈40 K. Other common semiconductor devices, the Si MOSFET and the GaAs MESFET, can operate over the entire cryogenic range, but they cannot yet match the extremely low noise levels of the Si JFET (1).

A number of Si JFETs are commercially available; however, as illustrated by reports since the 1960s, to obtain the lowest possible noise, commercial Si JFETs must usually be operated in the temperature range 100–200 K (2-17). Even though Si JFETs are above their "freeze-out" temperature and can function in the 50–100 K range, obtaining low

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noise in this range is difficult: their noise is significantly increased, sometimes exceeding that at room temperature, although there are exceptions. Also the cryogenic noise level often varies considerably among individual devices of the same type, requiring selection.

Commercial Si JFETs were considered for the low-temperature detector preamplifiers for the X-Ray Spectrometer (XRS) instrument which is slated to fly aboard the Japanese X-ray telescope Astro-E, as well as for readout of the cryogenic star-tracking telescope of the US satellite Gravity Probe B (GP-B) (18-20). The XRS required a noise voltage of <10 $nV/Hz^{1/2}$ in the frequency range 10 to 100 Hz at temperatures of 70 to 80 K; whereas for the GP-B telescope, a lower operating temperature is desirable and a somewhat higher noise level would be acceptable in exchange for lower input capacitance. We made low-frequency noise measurements on commercial Si JFETs of recent manufacture, including the Sony 2SK152, the InterFET NJ14AL and NJ30, and the Siliconix U440 (NNZ1 die), but in accord with the earlier reports, they showed noise levels higher than mission specifications in the required temperature ranges. Another drawback is that only certain gate sizes (and thus capacitances) are available.

Moreover, commercial Si JFETs are not designed with cryogenic applications in mind, and their fabrication may be discontinued, modified or transferred to other organizations, with potentially disastrous consequences to their cryogenic characteristics.

It would be extremely useful to have Si JFETs with input capacitance tailored to an application, and that dependably exhibit low noise below 100 K for applications requiring liquid-nitrogen (77 K) or liquid-argon temperature (87 K) operation. Furthermore, for other applications that require coupling the transistor to sensors operating at liquid-helium temperatures or down to the milli-Kelvin range, it would be useful to operate Si JFETs at the lowest possible temperature—at their operating limit of ≈40–50 K—to minimize power dissipation and heat input to the lower-temperature region of the sensor. The GP-B telescope is one such application, in which the JFETs are the active device for photodiode readout circuits that operate in an ≈2 K environment (20).

The difficulties of identifying and obtaining Si JFETs with suitable characteristics from commercial sources motivated us to undertake development and characterization of custom Si JFETs specially designed and fabricated for the liquid-nitrogen/liquid-argon temperature range. We describe the design and fabrication of these custom cryogenic Si JFETs, and report initial results from evaluations specifically directed toward their use in photodetector readout circuits for the GP-B telescope.

I. JFET Design & Fabrication

Analysis of the noise spectra from our measurements of commercial Si JFETs as a function of temperature over the range 70 to 130 K revealed an electron trap at ≈0.17 eV below the conduction band with a cross section of 1×10^{-14} cm^2. Examination of the literature indicated that the trap was possibly due to what is classically referred to as an "A centre" (21). The "A centre" has been studied extensively and is basically an oxygen

replacement of vacancies in the Si lattice. Further examination of the literature (most notably reference 22) led us to assume that these "A centre" defects probably formed during any high-temperature processing of the device. Classical methods of JFET processing involve a high-temperature (up to 1200°C) and long duration (several hours) P+ boron drive-in for conduction channel definition and device isolation. We decided to eliminate this P+ diffusion, as described below.

The basic fabrication of these cryogenic Si n-channel JFETs begins with P+ (boron 1 x 10^{19} cm^{-3}) (100) silicon wafers, 0.5 mm thick. On these wafers a high-quality 3 μm-thick epitaxial layer of N-type Si is grown (phosphorus 1 x 10^{16} cm^{-3}) (23). Note that this doping concentration is similar to that used for standard JFETs. The next fabrication step, and possibly the key to low noise, is an anisotropic etching of a channel-stop trench through the N-type epi into the substrate. This trench is etched approximately 4.5 μm deep using KOH solution, and has sloped side walls due to the anisotropy of the etching. By using this "trench" type mesa etching for device isolation rather than the traditional long-time/high-temperature P+ diffusion, we believe damage and defect formation are minimized.

The remaining processing steps are conventional: a P+ (boron) top gate diffusion and an N+ (phosphorus) source/drain ohmic contact diffusion. There are no implants for either of these steps, thus implant damage and annealing are avoided; this is another possible reason for good low-noise performance. The final step is an aluminum deposition for contacts and bond pads, followed by patterning and sintering. The JFET die were not metallized on the backside.

These cryogenic JFETs were designed with a range gate geometries: gate length from 2.5 to 12 μm, and gate width from 560 to 3250 μm.[c]

II. Measurements & Results

The following types of measurements were made:

(a) A limited evaluation of basic dc characteristics,

(b) Noise of individual JFETs,

(c) Gain and noise in various configurations of the readout circuit, although not operating in readout mode,

(d) Photon noise (photocurrent shot noise) and JFET noise during operation of the readout circuits in readout mode.

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[c]We use the conventional nomenclature: gate length is the gate dimension parallel to the channel current and gate width is the gate dimension perpendicular to the channel current. In this paper gate size is always given as length x width.

Measurement methods and results for each of the above types of measurements ar described below. Except for readout circuit T-4, as explained below, all individual FET or circuits were assembled onto TO-5 headers. In all cases the JFET die were attachec with silver epoxy; high-temperature eutectic die attach was avoided. For the cryogenic measurements the entire circuit (including the semiconductor die) was exposed and was immersed directly into liquid nitrogen. Even for the floating-gate noise measurements this direct immersion was practical, and measurements made with the circuits in the cold nitrogen gas above the liquid resulted in the same, or in some cases worse, noise. However, microphonics could be a problem, so it was necessary to avoid vibration or disturbances. The measurements were made with low power dissipation (~10–100 μW), in accord with the requirements for the GP-B readout. All noise spectra and figures of merit given in (b) and (c) below, are of noise voltage and are gate-referred (1).

*(a) **DC Characteristics*** DC characteristics were made using a Hewlett Packard 4145A Semiconductor Parameter Analyzer. The custom cryogenic JFETs exhibited excellent dc characteristics at liquid-nitrogen temperature, with the usual shift towards positive gate bias (towards zero) compared to room temperature, as shown in Figure 1 for a 12 μm x 2500 μm JFET.

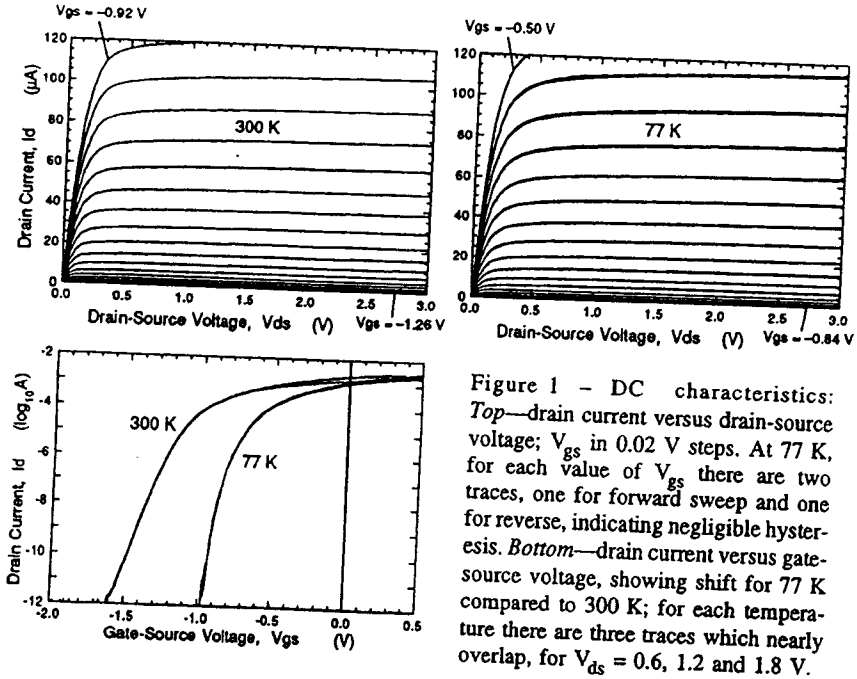

Figure 1 – DC characteristics: *Top*—drain current versus drain-source voltage; V_{gs} in 0.02 V steps. At 77 K, for each value of V_{gs} there are two traces, one for forward sweep and one for reverse, indicating negligible hysteresis. *Bottom*—drain current versus gate-source voltage, showing shift for 77 K compared to 300 K; for each temperature there are three traces which nearly overlap, for V_{ds} = 0.6, 1.2 and 1.8 V.

(b) Noise of Individual JFETs An example of the liquid-nitrogen shorted-gate noise-voltage spectrum for an individual 12 μm x 2500 μm JFET (Figure 2) illustrates the excellent noise level, with $K_f \equiv A_f$ x gate area ≈ 8 $\mu V^2 \cdot \mu m^2$ (1) for a power dissipation of only 60 μW in the JFET.

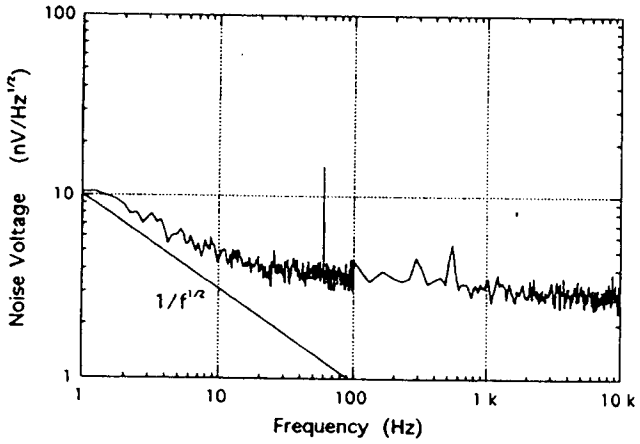

Figure 2 – Shorted-gate, gate-referred noise-voltage spectrum for a 12 μm x 2500 μm gate custom cryogenic Si JFET at 77 K; I_d = 50 μA, V_{ds} = 1.2 V (g_m ≈ 0.6 mS).

(c) Gain and Noise of JFETs in Readout-Circuit Configuration The photodiode readout circuit used for these evaluations is shown in Figure 3, in which a custom Si JFET is used as the buffer FET. During operation the photodiode current is integrated on the combined capacitance of the photodiode, buffer JFET gate, reset FET, compensation capacitor C and any stray capacitance. As the charge accumulates, a voltage ramp is output, with slope proportional to the photocurrent, I_p.

However, for the measurements described in this section this circuit was not operated in readout mode. First, shorted-gate noise measurements were made on the buffer JFET using direct connections; to access the gate a temporary bond wire shorted the compensation capacitor, C. The gain and noise were measured by using two different circuits: (1) grounded source, with V_{ds} fixed, as described in reference (24), and (2) source-follower. Subsequently, the temporary bond wire was removed to allow the JFET gate to "float", and the gain and noise measurements were repeated at liquid-nitrogen

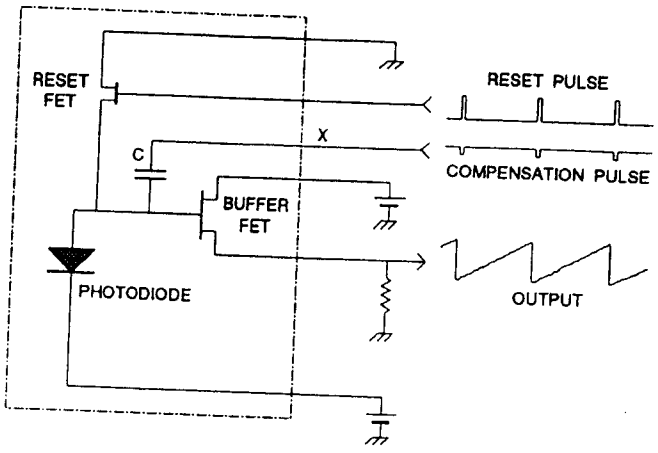

Figure 3 – Basic readout circuit being evaluated in these measurements. The portion within the dashed line operates at cryogenic temperature.

temperature only. In both cases a test signal was fed into point "X" for the gain measurements, and point "X" was grounded for the noise measurements. The reset FET was turned off for all these measurements. Circuit operation in the floating-gate mode was verified by using the photodiode as an isolated current source, and repeating the measurements after integrating charge onto the JFET gate by momentarily illuminating the photodiode. Comparison of the gains between the shorted-gate and floating-gate measurements allowed an estimate of the circuit capacitance as well as the JFET gate-to-source capacitance, since the capacitance of C was known (3 to 7 pF, depending on the circuit).

Such measurements were made on three readout circuits having different size JFETs. The noise-voltage spectra for readout circuit NB-1 having the smallest JFET (5 μm x 560 μm) are shown in Figure 4. For all measurements the JFET power dissipation was approximately 16 μW (V_{ds} = 1.2 V, $I_d \approx 13$ μA, $g_m \approx 0.24$ mS) and V_{gs} was approximately 1 V. Figure 4 shows good agreement among the spectra for the various circuit configurations; the source-follower floating gate spectrum has been divided by the appropriate input capacitance ratio, $(C_{gs} + C_{total})/C_{total} \approx 2.0$ for this circuit, where C_{gs} is the buffer FET gate-to-source capacitance and C_{total} is the total input capacitance. Similar results (but with lower noise) were obtained for the other two circuits, having larger JFETs.

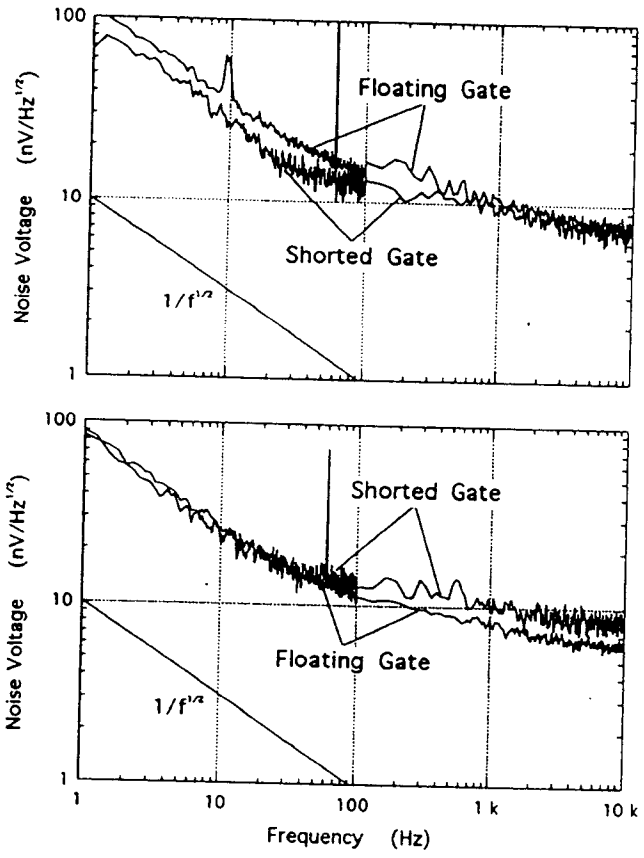

Figure 4 - Noise-voltage spectra at 77 K for a 5 μm x 560 μm gate Si JFET in a readout circuit (Figure 3): *Top*—for grounded-source measurement circuit. *Bottom*—for source-follower measurement circuit. All four noise spectra are in good agreement.

(d) Noise during Readout Operation of Readout Circuits The output voltage ramps from two readout circuits were collected during readout operation at cryogenic temperature under conditions approximating the projected operating conditions for the GP-B telescope. Both circuits used the 5 μm x 560 μm gate JFET. The circuits were operated inside a vacuum can during the measurements: for circuit NB-1 (the same circuit described in (c) above), built directly on a TO-5 header, the vacuum can was immersed in liquid nitrogen; whereas for circuit T-4, built on a thermal isolation platform and heated with a power of approximately 200 μW (≈40 μW in the FET, the remainder in a heater resistor), the vacuum can was immersed in liquid helium (25). The results for circuit NB-1, with and without illumination on the photodiode, are shown in Figure 5; the left-hand plots are the slopes of 400 successive integration ramps output by the readout circuit,[d] and the right-hand plots are histograms of the distribution of the 400 slopes. Table 1 summarizes the results for both readout circuits.

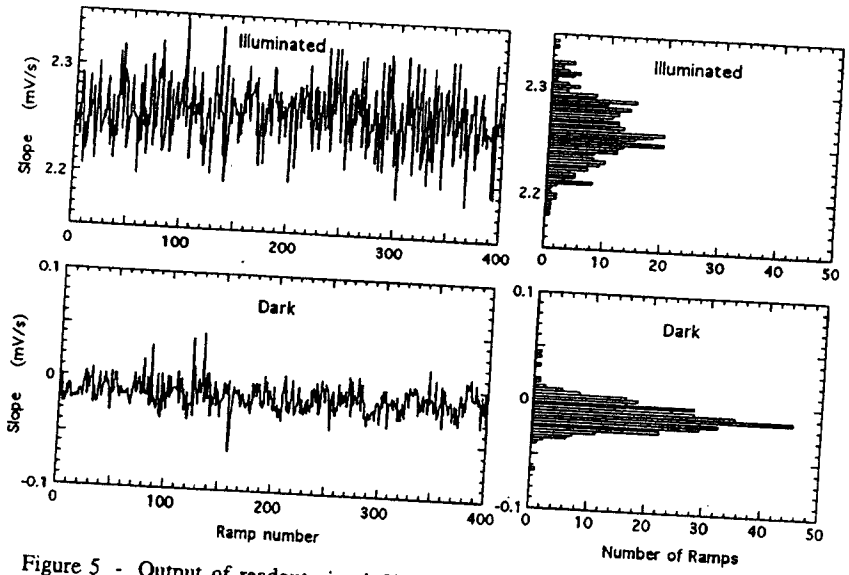

Figure 5 - Output of readout circuit NB-1 operating at 77 K with 0.1 seconds between resets: *Top*–with illumination generating ≈15 fA photocurrent, showing photon (shot) plus preamplifier noise. *Bottom*–without illumination, showing preamplifier (JFET) noise only. Slopes of the output ramps are plotted on the left and corresponding histograms of the distribution of the slopes are on the right.

[d]The readout circuit outputs were passed through a 1 kHz filter and then sampled at 4 kHz; the slope of each ramp was determined as a least squares fit to 320 sampled points along the ramp.

Standard deviations derived from the data plotted in Figure 5 for photon (shot) noise (subtracting the JFET noise, right-most column in Table 1) are in reasonable agreement with those calculated from shot-effect statistics (column 4), $\Delta I_p = (eI_p/\Delta t)^{1/2}$. An integration capacitance, C_i, of ≈6.5 pF determined as described in section (c) is used to calculate the photocurrent, $I_p = C_i \times$ slope. Also, the JFET noise is comparable to the photon noise for both circuits. The photodetector is assumed to be noiseless at the cryogenic temperatures.

Table 1 - Readout circuit characteristics: second column is the average slope of the 400 ramps as plotted is Figure 5 (illuminated); the corresponding average photocurrent is given in column 3; columns 4 and above are standard deviations given in mV/s and in fA.

Readout circuit	Average slope (mV/s)	Average photocurrent, i_p (fA)	Calculated shot noise	Total measured noise (illuminated)	Measured JFET noise (dark)	Net measured shot noise
NB-1	2.26	15	0.024/0.16	0.028/0.18	0.0115/0.075	0.026/0.17
T-4	1.15	7.5	0.017/0.11	0.017/0.11	0.0084/0.055	0.015/0.098

III. Summary/Conclusions

By means of custom fabrication, we have made Si JFETs that exhibit excellent low-frequency noise at temperatures for which the noise of commercial JFETs has typically risen to undesirable levels. These custom JFETs are thus suited for applications where it is desirable that circuits operate at temperatures in the liquid-nitrogen/liquid-argon range, or at as low a temperature as possible, down to the operating limit of Si JFETs. We attribute their cryogenic performance to special attention to design and fabrication procedures. The JFETs were evaluated for use in readout circuits for photodiodes for the Gravity Probe B telescope, but the results are applicable to other applications.

These cryogenic JFETs were found to exhibit K_f values at 77 K between ≈8 and ≈20 $\mu V^2 \cdot \mu m^2$ at low drain current (≈10–50 μA). This compares favorably with recent reports of measurements near this temperature for commercial Si JFETs giving K_f ≈25 and ≈140 $\mu V^2 \cdot \mu m^2$ (16,17). Also we found that floating-input noise corresponded to shorted-input noise, thus gate-referred noise current was not measurable, as expected.

The measurements of most interest for the GP-B telescope are those of readout circuits, and the noise values for different circuits and measurement configurations agree with one another as predicted from analysis of the circuits and values of capacitance calculated from gain measurements.

IV. ACKNOWLEDGEMENTS

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