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Gravity Probe B Relativity Mission

BOARD-LEVEL TEST PROCEDURE FOR THE GYROSCOPE SUSPENSION SYSTEM (GSS) ACU AFT BACKPLANE (ABP) BOARD

PWA 8A01901 Rev D **S/N:** ☐

GP-B Procedure
P0596 Rev B

Prepared by: Scott Smader — Date
RE, ABP

Approved by: William Bencze — Date
RE, Gyroscope Suspension System (GSS) Group

Approved by: Dorrene Ross — Date
GP-B Quality Assurance

Table of Contents:

1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this test procedure	29-Feb-00	S Smader
A0	Replace ADDA procedure by Flt Cmd 16,1,0x20E	3-Mar-00	S Smader
A1	Clarify software commands. Clarify tolerance for ringing of APU clocks	4-Apr-00	S Smader
A2	Change Pre-Insertion Static Tests to Post-Insertion Static Tests; clarify Monitors test	6-Apr-00	S Smader
A	Second release	7-Apr-00	S Smader
B	Updates after current sensor repair	17-May-00	S Smader

2.0 Scope:

This procedure details the board-level electrical functional tests on the GSS Aft Backplane (ABP) card. No mechanical or thermal stress testing shall be performed at this time.

This test plan has been written to be run with the GSS "Gold System" test fixture – an electrically and interface equivalent of the GSS flight units. In General, the Device Under Test (DUT) shall be inserted into the Gold System in place of the equivalent Gold System card, any additional electrical connections to the Gold System shall be made, and a set of software-based and possibly manual tests will be run on the board. Upon successful completion of this procedure, this board is considered electrically functional.

All data recorded during this test is recorded in this document; each test of a board will use its own copy of this procedure, and will be identified by serial number in the upper right corner.

3.0 Reference Documents

3.1. GSS Gold System Hardware and Software Configuration Standard, P0663

3.2. PWA Drawing, GSS Aft Backplane board, 8A01901

3.3. PWB Drawing, GSS Aft Backplane board, 8A01873

3.4. Board-level test software operational procedure, P0670

3.5. Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment, MIL-STD-1686

4.0 Test Facilities

HEPL Room 127, Stanford University

5.0 QA Provisions:

5.1. This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the ONR representative (E. Ingraham) shall be notified 24 hours prior to he start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

Date/time:_____	Date/time:_____
GP-B QA (D. Ross)	ONR (E. Ingraham)

5.2. Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

6.0 Test Personnel

This test procedure is to be conducted only by the following certified personnel:

6.1. William Bencze

6.2. Scott Smader

6.3. Joe Kilner

6.4. Lo Van Ho

7.0 General Instructions

7.1. Redlines can be initiated by the certified test personnel listed in Section 6.0 and must be approved by QA.

7.2. Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.

7.3. Any nonconformance or test anomaly should be reported by a Discrepancy Report. Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.

7.4. Only the following persons have the authority to exit/terminate this test or perform a retest: Certified test operators listed in Section 6.0 and GP-B QA.

7.5. In this document, “Perform Flight S/W system test commands:” means to prepare the test system software as described in P0670 Board-Level Test Software Operational Procedure, and then issue the listed commands according to the procedure described in P0670.

8.0 Hardware Safety Requirements:

8.1. This assembly is ESD sensitive; special care shall be exercised per the “Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment”, MIL-STD-1686

8.2. Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

8.3. Examine all mating connectors before attempting to mate them. Remove any foreign particles. Look for any damaged pins or sockets. Do not force the coupling action if excessive resistance is encountered. Ensure that key-ways are aligned when mating connectors.

9.0 Equipment Pretest Requirements:

9.1. The GSS Gold System in which this board is to be tested must have passed successfully the P0663 – Gold System Certification Procedure prior to the start of this test. Record the Gold System serial number and date of its certification, below.

GSS Gold System	SN:	
	Date of Certification	
	Configuration (circle one)	Full Partial

10.0 Additional Test Equipment

The following support hardware, test equipment, or software will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list as needed.

Equipment Description	Make	Model	SN	Cal Due
1. Oscilloscope	Tektronix			
2. 2 ea BNC coax cables				
3. Digital Multimeter	Fluke			
4.				
5.				
6.				

11.0 Device Under Test (DUT):

Record the serial number of the Device Under Test, or DUT.

PWA 8A01901 GSS Aft Backplane	SN:	

Test Operator:	Name:	

Start of test:	Date, Time	

12.0 Pre-test visual inspection.

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

		P/F	Notes
12.1.	Remove PWA from storage container.		
12.2.	Verify that no parts are missing, unless called out in the assembly drawing.		
12.3.	Verify that the following capacitors are installed in the proper orientation: C1, C2, C3, C4.		
12.4.	Verify the proper orientation of pin 1 of all DIP packages: U1, U2, U3, U4.		

13.0 Post-Insertion Static Electrical Tests:

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

13.1. Board installation:

	P/F	Notes
13.1.1. Install PWA in gold system enclosure per the instructions in P0663 – Gold System certification procedure. Do not yet install other PWAs.		

13.2. Power circuits isolation check

A. Set meter to “ohms”, record indicated resistance between the indicated pins.

B. With all power off, ensure that Power Cable between APU and DUT is not installed.

	P/F	Notes
13.2.1. TP1 DGND to TP6 P5V		Value:
13.2.2. TP1 DGND to TP5 P3.3V		Value:
13.2.3. TP1 DGND to TP4 M15V		Value:
13.2.4. TP1 DGND to TP3 P15V		Value:
13.2.5. TP6 P5V to TP5 P3.3V		Value:
13.2.6. TP6 P5V to TP4 M15V		Value:
13.2.7. TP6 P5V to TP3 P15V		Value:
13.2.8. TP6 P5V to TP7 AGND		Value:
13.2.9. TP5 P3.3V to TP4 M15V		Value:
13.2.10. TP5 P3.3V to TP3 P15V		Value:
13.2.11. TP5 P3.3V to TP7 AGND		Value:
13.2.12. TP4 M15V to TP3 P15V		Value:
13.2.13. TP4 M15V to TP7 AGND		Value:
13.2.14. TP3 P15V to TP7 AGND		Value:
13.2.15. TP1 DGND to TP7 AGND.		Value:

DUT passes this section if all measurements are greater than 100k ohms.

Board S/N:

13.3. Power cable installation:

Note: Connect only the APU cable at this time. Do not install other PWAs at this time.

	P/F	Notes
13.3.1. Cable system for "Configuration B" per P0663 – Gold System certification procedure		

13.4. Power circuits connection check:

A. Set meter to "ohms", record indicated resistance between the indicated pins.
B. With all power off, ensure that Power Cable between APU and DUT is installed. Leave cable connected and power off during the following tests. Check for short circuit between each two points, i.e., less than 2.0 ohms. Subtract lead resistance if significant.

	P/F	Notes
13.4.1. TP1 DGND to TP7 AGND		Value

DUT passes this section if all measurements are less than 2.0 ohms.

14.0 In-System Testing – Flight Configuration

Note: Tests run in this section are run with the hardware in "flight" configuration: no external test equipment or cables. The tests here use only the onboard diagnostic facilities of the GSS hardware. These will be the equivalent of the on-orbit tests of this system.

14.1. Board installation:

	P/F	Notes
14.1.1. Install PWA in gold system enclosure per the instructions in P0663 – Gold System certification procedure		
14.1.2. Cable system for "Configuration B" per P0663 – Gold System certification procedure		

14.2. System Functional Tests:

	P/F	Notes
14.2.1. Perform Flight S/W system test commands: 14 1 14 38 Record 'Pass' if the command is successful. Otherwise record 'Fail' *Tests: Full GFAB data paths*		
14.2.2. Perform Flight S/W system test commands: 14 1 14 201 If the value of "PIT 3-diag. Monitors", "Monitor 3:" is 0x0001, record 'Pass' for this test. Otherwise record 'Fail'. *Tests: Routing of 16f0 clock*		
14.2.3. Perform Flight S/W system test commands: 14 1 14 29 Record results. *Tests: EBI bus.*		
14.2.4. Perform Flight S/W system test commands: 16 100 16 2 0x0101 20 1 1 16 2 0x0100 7 16 1 0x020E If the value of "PIT 3-diag. Monitors", "Monitor 3:" is 0x0003, record 'Pass' for this test. Otherwise record 'Fail'. *Tests: Routing of clocks*		

DUT passes this section if all tests above are "Pass".

15.0 In-System Testing – Ground Test Configuration

Note: Tests run in this section require the addition of test cables and external test hardware. They are used to verify the board functioning of the board in fine detail, and are only used at the time of board-level test and acceptance. These may be considered "Engineering Confidence Tests".

15.1. Power Supplies:

With an APU or equivalent connected via J12, with nothing installed in J61 through J66, and with power applied, set meter to "volts dc", and record the following Power Supply voltages. Note the polarity for meter hookup.

	Min	Max	P/F	Notes
15.1.1. TP6 P5V (+) relative to TP1 DGND (-).	4.75 V	5.25 V		Measurement:
15.1.2. TP5 P3.3V (+) relative to TP1 DGND (-).	3.135 V	3.465 V		Measurement:
15.1.3. TP4 M15V (-) relative to TP7 AGND (+).	13.5 V	16.5 V		Measurement:
15.1.4. TP3 P15V (+) relative to TP7 AGND (-).	13.5 V	16.5 V		Measurement:
15.1.5. TP1 DGND (+) relative to TP 7 AGND (-).	-0.1 V	+0.1 V		Measurement:

DUT passes this section if all measured values are within the listed ranges.

15.2. APU Clocks:

This test requires the use of an APU Simulator with P/N PC640 to monitor APU cable pins 3, 2, 16, and 15, which are labeled on the APU simulator unit as:

Unit #1 Label	APU Pin #
Custom Sync +, 136 kHz	3
Custom Sync -, 136 kHz	2
Custom Sync +, 545 kHz	16
Custom Sync -, 545 kHz	15

Note the results of this test in the table below.

A. Configure the oscilloscope with Timebase A set to Chop, monitor APU pin 3 (Custom Sync +, 136 kHz) and APU pin 2 (Custom Sync -, 136 kHz).

B. Trigger on the rising edge of the signal on APU pin 3 (Custom Sync + 136 kHz).

C. For each trace, confirm that the signals are mutually synchronous and that the voltage swings between DGND and P5V (minor overshoots and/or significant ringing allowed) at approximately 136 KHz. Confirm that the signal on APU pin 2 (Custom Sync -, 136 kHz) is the inverse of the signal on APU pin 3 (Custom Sync +, 136 kHz).

D. Disconnect APU pin 3 (Custom Sync + 136 kHz) and APU pin 2 (Custom Sync -, 136 kHz).

E. Using an oscilloscope with Timebase A set to Chop, monitor APU pins 16 (Custom Sync +, 545 kHz) and 15 (Custom Sync -, 545 kHz). Trigger on the rising edge of the signal on APU pin 16 (Custom Sync +, 545 kHz).

F. For each trace, confirm that the signals are mutually synchronous and that the voltage swings between DGND and P5V (minor overshoots and/or significant ringing allowed) at approximately 545 KHz. Confirm that the signal on pin APU 16 (Custom Sync +, 545 kHz) is the inverse of the signal on APU pin 15 (Custom Sync -, 545 kHz).

Assertion	P/F	Notes
15.2.1. Pins 3 and 2 are mutually synchronous		
15.2.2. Voltage swings between DGND and P5V		
15.2.3. Frequency approximately 136 KHz		
15.2.4. Pin 2 is inverse of Pin 3		
15.2.5. Pins 16 and 15 are mutually synchronous		
15.2.6. Voltage swings between DGND and P5V		
15.2.7. Frequency approximately 545 KHz		
15.2.8. Pin 16 is inverse of Pin 15		

If all of the above assertions are confirmed, the DUT passes.

15.3. Monitors Test:

This test requires the use of Configuration B per P0663 to confirm the routing of various power supply and temperature monitors

15.3.1. Board installation:

		P/F	Notes
15.3.1.1.	Install PWA in gold system enclosure per the instructions in P0663 – Gold System certification procedure		
15.3.1.2.	Cable system for "Configuration A" per P0663 – Gold System certification procedure		

15.3.2. Test Monitors:

After power has been applied for at least 5 minutes to allow ambient temperature to stabilize and thermal sensors to reach ambient temperature, run AMT Diagnostics as described in P0597, sections 15.5 and 15.6. Record and calculate the following information.

AMT-monitored Signal		"Min"	"Max"	P/F	Min	Max
15.3.2.1.	APUPMONB	FF00	00FF			
15.3.2.2.	APUPMONA	BF00	C100			
15.3.2.3.	+15 V / 2	5FC0	5FFF			
15.3.2.4.	–15 V / 2	9FC0	A040			
15.3.2.5.	AGND	FFF0	0010			
15.3.2.6.	+5 V	3FB0	3FFF			
15.3.2.7.	+3.3 V	2A90	2AE0			
15.3.2.8.	APU TEMP MON (1)	0E00	0F00			
15.3.2.9.	R6K TEMP MON (2)	Record value:				
15.3.2.10.	AMT TEMP MON (1)	2500	26FF			
15.3.2.11.	ATC TEMP MON (1)	2500	26FF			
15.3.2.12.	ACU TOTAL CURRENT (2)	Record value:				
15.3.2.13.	R6K CURRENT (2)	Record value:				
15.3.2.14. (2)	ACS CONTROL EFFORT	Record Value				

(1) Measured values outside of range may be acceptable depending on ambient temperature according to the discretion of the test director.

(2) Only record value for engineering use: no pass/fail criteria.

Note: Some of the values in the table include two's-complement, negative hexadecimal numbers. For measurements close to zero volts, i.e., APUPMONB and AGND, the ranges wrap around zero. For these ranges and for ranges (measurements) that are wholly positive, "Min" and "Max" have the correct meanings. For ranges (measurements) that are wholly negative, i.e., APUMONA and –15 V / 2, however, the labels "Min" and "Max" need to be considered as unsigned numbers for the labels to be accurate. The purpose of this subtlety is supposed to be to make performing the test more straightforward. This Note is here only to clarify any question that might arise about whether the "Min" value is less than the "Max" value.

DUT passes this section if all measured values are between indicated Min and Max values.

Board S/N:

16.0 Completion of Procedure:

		P/F
16.1.	Turn off power to FSU and ACU enclosures.	
16.2.	Remove PWA from enclosure per P0663 and return to storage container.	

Notes

I certify that this procedure was performed in whole and that the data recorded above is complete and accurate.

Test Engineer | Date

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative | Date

Quality Assurance | Date