W. W. Hansen Experimental Physics Laboratory
STANFORD UNIVERSITY
STANFORD, CALIFORNIA 94305 - 4085

Gravity Probe B Relativity Mission

BOARD-LEVEL TEST PROCEDURE FOR THE GYROSCOPE SUSPENSION SYSTEM (GSS) AFT CLOCK SUPPORT (ACS) BOARD

PWA 8A01898 Rev C **S/N:** [ ]

GP-B Procedure
P0598 Rev A

Prepared by: Joseph R. Kilner Date

Approved by: William J. Bencze Date
RE, Gyroscope Suspension System (GSS) Group

Approved by: Dorrene Ross Date
GP-B Quality Assurance

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1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this test procedure	3-Mar-00	JR Kilner
A	Updated based on dry-runs on gold system hardware	27-Mar-00	JR Kilner

2.0 Scope:

This procedure details the tests required to perform board-level electrical functional tests on the GSS Aft Clock Support (ACS) card. No mechanical or thermal stress testing shall be performed at this time.

This test plan has been written to be run with the GSS "Gold System" test fixture – an electrically and interface equivalent of the GSS flight units. In General, the board under test shall be inserted into the gold system in place of the equivalent gold system card, any additional electrical connections to the gold system shall be made, and a set of software-based and possibly manual tests will be run on the board. Upon successful completion of this procedure, this board is considered electrically functional.

All data recorded during this test is recorded in this document; each test of a board will use its own copy of this procedure, and will be identified by serial number in the upper right corner.

3.0 Reference Documents

3.1. GSS Gold System Hardware and Software Configuration Standard, S0663

3.2. Aft Clock Support tuning procedure, P0666

3.3. PWA Drawing, GSS Aft Clock Support board, 8A01898

3.4. PWB Drawing, GSS Aft Clock Support board, 8A01874

3.5. Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment, MIL-STD-1686

4.0 Test Facilities

HEPL Room 127, Stanford University.

5.0 QA Provisions:

5.1. This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the ONR representative (E. Ingraham) shall be notified 24 hours prior to he start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

Date/time:_____ Date/time:_____

GP-B QA (D. Ross) ONR (E. Ingraham)

5.2. Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

6.0 Test Personnel

This test procedure is to be conducted only by the following personnel:

6.1. William Bencze

6.2. Scott Smader

6.3. Joe Kilner

6.4. Lo Van Ho

7.0 General Instructions

7.1. Redlines can be initiated by the test personnel listed in Section 6.0 and must be approved by QA.

7.2. Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.

7.3. Any nonconformance or test anomaly should be reported by a Discrepancy Report. Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.

7.4. Only the following persons have the authority to exit/terminate this test or perform a retest: Test operators listed in Section 6.0 and GP-B QA.

8.0 Hardware Safety Requirements:

8.1. This assembly is ESD sensitive; special care shall be exercised per the "Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment", MIL-STD-1686

8.2. Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

8.3. Examine all mating connectors before attempting to mate them. Remove any foreign particles. Look for any damaged pins or sockets. Do not force the coupling action if excessive resistance is encountered. Ensure that key-ways are aligned when mating connectors.

9.0 Equipment Pretest Requirements:

9.1. The GSS Gold System in which this board is to be tested must have passed successfully the P0663 – Gold System Certification Procedure prior to the start of this test. Record the Gold System serial number and date of its certification, below

GSS Gold System	SN:	
	Date of Certification	
	Configuration (circle one)	Full Partial

9.2. This board must have undergone P0666, ACS Card Tuning Procedure prior to this test.

10.0 Test Equipment

The following support hardware, test equipment, or software will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list may be made in the spaces provided.

Equipment Description	Make	Model	SN	Cal Due
1. GSS Gold System (partial or full)				
2. Digital Multimeter	Fluke			
3. Digital Oscilloscope with probes	Tektronix			
4. Analog Oscilloscope with probes	Tektronix			
5. PC with PC-EBI interface card and cable	-	-		NR
6. SRE Clock simulator	-	-		NR
7. Programmable clock generator	Stanford Research Systems (SRS)			
8. PC355 Test card				NR
9.				
10.				

11.0 Device Under Test (DUT):

Record the serial number of the board under test (ie, Device Under Test, or DUT).

PWA 8A01898C GSS Aft Clock Support	SN:	
Test Operator:	Name:	
Start of test:	Date: Time:	

12.0 Pre-test visual inspection.

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected a an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

		P/F	Notes
12.1.	Remove PWA from storage container.		
12.2.	Verify that no parts are missing, unless called out in the assembly drawing.		
12.3.	Verify the proper orientation of pin 1 of all DIP packages: All DIPs have pin 1 farthest from the 120-pin connector.		
12.4.	Verify that D1, D2, and D3 have been installed with the correct orientation.		
12.5.	Verify that Q1 is installed with the correct orientation.		
12.6.	Verify that tuning procedure P0666 has been performed on this board and that the proper value of C13 is installed. Record installed value of C13 at the right.		Value of C13:

13.0 Pre-Insertion Static Electrical Tests:

Note: All handling of this PWA shall be performed using ESD control methods, as outlined MIL-STD-1686. Unit shall be inspected a an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

13.1. Power circuit isolation check

Set meter to "ohms", record indicated resistance between the indicated pins. Note the polarity for meter hookup.

Pass/Fail criterion: DUT passes if all resistance measurements are > 100 kohms.

	P/F	Notes
13.1.1. (+) to P2 pin 120 [Vcc] ↔ (-) to P2 pin 2 [AGND]		Measurement: Ohms.
13.1.2. (+) to P2 pin 1 [P15V] ↔ (-) to P2 pin 118 [DGND]		Measurement: Ohms.
13.1.3. (+) to P2 pin 118 [DGND] ↔(-) to P2 pin 3 [M15V]		Measurement: Ohms.

14.0 In-System Testing – Flight Configuration

Note: Tests run in this section are run with the hardware in "flight" configuration: no external test equipment or cables. The tests here use only the onboard diagnostic facilities of the GSS hardware. These will be the equivalent of the on-orbit tests of this system.

This section not applicable

15.0 In-System Testing – Ground Test Configuration

Note: Tests run in this section require the addition of test cables and external test hardware. They are used to verify the board functioning of the board in fine detail, and are only used at the time of board-level test and acceptance. These may be considered "Engineering Confidence Tests".

15.1. Board installation:

		P/F	Notes
15.1.1.	Install PWA in gold system enclosure per the instructions in P0663 – Gold System certification procedure		
15.1.2.	Cable system for "Configuration A" per P0663 – Gold System certification procedure (PC-EBI)		

15.2. Test Equipment Setup.

		P/F
15.2.1.	Connect the Function Generator output (Function output) to the Ext 16f0 A input of the Clock Emulator.	
15.2.2.	Connect the 16f0 A output of the Clock Emulator to channel 1 of the digital oscilloscope through a co-ax.	
15.2.3.	Connect the FPGA_DIAG monitor (pin 21 of the 25-pin connector on the Test Fixture) to channel 2 of the digital oscilloscope using a 10:1 probe. (Connect all of the probe grounds to pin 13.)	
15.2.4.	Connect the APU clock (via BNC on Aft power supply module) to channel 3 of the digital oscilloscope using a 10:1 probe.	
15.2.5.	Connect INT0 (pin 25 of the 25-pin connector on the Test Fixture) to channel 4 of the digital oscilloscope using a 10:1 probe.	
15.2.6.	Connect INT1 (BNC connector on the Test Fixture) to channel 1 of the analog oscilloscope.	
15.2.7.	Connect INT2 (BNC connector on the Test Fixture) to channel 2 of the analog oscilloscope.	
15.2.8.	Connect INT3 (pin 11 of the 25-pin connector on the Test fixture) to channel 3 of the analog oscilloscope.	

	P/F	Notes
15.2.9. Function Generator settings: A. Select square wave, B. frequency = 16.368000 MHz, C. Ampl = 4.60V, D. Offset = 2.50V, E. leave display on 'frequency' with step size = 100.		
15.2.10. GSS-SRE Clock Emulator switch settings: A. ON; 10Hz A, 16fo A, Ext 16fo. B. OFF; 10Hz B, 16fo B, Ext 10Hz.		

15.3. Digital Scope Setup:

	P/F
15.3.1. Vertical Menu: Position; place channel one at the top followed by channels two, three, and four; Scale; set to 5V per cm (may indicate 500mV per cm if scope does recognize the probe as a 10:1 probe); set all channels to full bandwidth and DC coupling	
15.3.2. Horizontal Menu: Select Main Time Base, set Trigger Position = 50%, Set Record Length = 1000, (if available on scope) set Fit-to-screen = OFF (in Extd Acq Setup)	
15.3.3. Trig Menu: Type = edge, Source = Channel 4, Coupling = DC, Slope = rising, Level = about half of max (250mV), set to Auto Trig, set Holdoff = minimum	
15.3.4. Acquire Menu: Mode = Hi Res, Repetitive Signal = OFF (or ON for a lower sampling frequency scope), Stop After = R/S button, Limit test = OFF	
15.3.5. Measure the frequencies of channels one, two, and three – setup these measurements in this order	
15.3.6. When running, press the "Clear Menu" button to achieve an uncluttered display	
15.3.7. Use a sweep speed of 100 nsec per cm or slower depending on the signal of interest	

15.4. Test Software

Notes on the test software display:

The top line of the display contains a 16-bit (4 Hex characters) counter incrementing at about 20 counts per second whenever the program is running. Following two lines of labels, the next line displays the data that the program is writing to registers 0, 1, 4, and 5 on the AMT board. The next line lists the data read back from the same four registers plus five status bits read from the PC_EBI board.

Except for the status bits that are displayed in binary, all displays are 16-bit words displayed in Hex. In Hex, 4 bits (representing the decimal values from 0 to 15) are displayed as 0 … 9, a, b, c, d, e, f where a = 10, f = 15, etc. The right character of the Hex word is formed from the four LS bits (3, 2, 1, and 0); the next Hex character is formed from bits 7, 6, 5, and 4; etc.

The read-back data should be the same as the written data except as follows:

A. *If the right two nibbles of Reg 0 consist of only 0's and/or 7's, 0080 is added to the Reg 0 read back;*
B. *The MS bit of Reg 1 is INT4 (this is the internally generated equivalent of INT0);*
C. *The two bits represented by 8800 in Reg 4 are the latched and unlatched readings of the AMT diagnostic Mux whenever it is enabled;*
D. *The right byte of Reg 5 is read back in the left byte; and the right nibble of Reg 5 is the input-only PPin (bit 7 is the ADC latchup flag.*

The status bits are latched on the PC_EBI board as they occur. The status, flag, and INT4 bits are cleared under program control just after they are read. It is normal for the DACK status bit to remain at zero.

Next shown are the 16 A-to-D converter readings along with their labels.

The last line of the display lists the test number and a short description of the test.

15.5. APU Clock tests:

		Range	P/F	Notes
15.5.1.	Execute test code “T1.exe”.			
15.5.2.	Verify the frequency of the pair of high-frequency APU clocks at aft PS module BNC connectors	545.6 kHz ± 5 kHz		Measured freq:
15.5.3.	Verify the pair of high-frequency APU clocks are of opposite phase at aft PS module BNC connectors.			
15.5.4.	Verify the frequency of the pair of low-frequency APU clocks at aft PS module BNC connectors	136.4 kHz ± 2 kHz		Measured freq:
15.5.5.	Verify the pair of low-frequency APU clocks are of opposite phase at aft PS module BNC connectors.			

15.6. PLL Lock range tests:

Pass/Fail Criteria: The PLL is locked whenever the PLL Control Effort is between 0x1000 and 0x7000.

		P/F	Notes
15.6.1.	Set frequency generator to 16.367500 MHz; verify PLL remains locked. Record PLL control effort		Meas Ctrl Effort
15.6.2.	Set frequency generator to 16.368000 MHz; verify PLL remains locked. Record PLL control effort		Meas Ctrl Effort
15.6.3.	Set frequency generator to 16.368500 MHz; verify PLL remains locked. Record PLL control effort		Meas Ctrl Effort

15.7. SRE input clock selection tests:

For the given 16fo input clock settings on the SRE emulator, confirm that the right nibble of Reg5 display is the given value:

	16 fo A	16 fo B	Expected Reg5 right nibble	P/F	Measured Reg5 right nibble
15.7.1. Clock settings:	0	0	C		
15.7.2. Clock settings:	1	0	D		
15.7.3. Clock settings:	0	1	E		
15.7.4. Clock settings:	1	1	F		

0 = clock off; 1 = clock on (1's shaded for clarity)

15.8. SRE 10Hz clock selection test:

The 10 Hz is indicated ON (1) when the Int0 bit of the status word is flashing.

	10 Hz A	10 Hz B	16 fo A	16 fo B	Expected 10 Hz indication	P/F
15.8.1. Clock settings:	0	0	0	0	0	
15.8.2. Clock settings:	1	0	0	0	0	
15.8.3. Clock settings:	0	1	0	0	0	
15.8.4. Clock settings:	1	1	0	0	0	
15.8.5. Clock settings:	0	0	1	0	0	
15.8.6. Clock settings:	1	0	1	0	1	
15.8.7. Clock settings:	0	1	1	0	0	
15.8.8. Clock settings:	1	1	1	0	1	
15.8.9. Clock settings:	0	0	0	1	0	
15.8.10. Clock settings:	1	0	0	1	0	
15.8.11. Clock settings:	0	1	0	1	1	
15.8.12. Clock settings:	1	1	0	1	1	
15.8.13. Clock settings:	0	0	1	1	0	
15.8.14. Clock settings:	1	0	1	1	1	
15.8.15. Clock settings:	0	1	1	1	0	
15.8.16. Clock settings:	1	1	1	1	1	

0 = clock off; 1 = clock on (1's shaded for clairty)

15.9. Test Series T1:

Equipment Setup:

	P/F	Notes
15.9.1. Restore the SRE Clock Emulator switches to the following settings: ON; 10Hz A, 16fo A, Ext 16fo. OFF; 10Hz B, 16fo B, Ext 10Hz.		
15.9.2. Set the scope horizontal sweep to 100 nsec/cm. Adjust the horizontal position so that a rising edge of the16fo clock is on the scope centerline.		

Perform the following four tests:

A. Check all registers; the output registers should be the same as the input registers except as noted above.
B. Determine the presence of the APU clocks; use either one of the two APU clocks
C. Determine the presence of the SRE 16f0 clock. When present, the scope will remain in sync and the PLL control effort will remain within the lock range.
D. Check the phase of the16f0 clock. Is the phase normal with the rising edge on the scope centerline or is it inverted with the falling edge on the centerline?

	P/F	Notes
15.9.3. Execute test code “T1.exe”.		
15.9.4. Check registers (Test A)		
15.9.5. Verify APU clock on (Test B)		
15.9.6. Verify SRE clock on (Test C)		
15.9.7. Verify phase is “normal” (Test D)		

	P/F
15.9.8. Execute test code “T1a.exe”.	
15.9.9. Check registers (Test A)	
15.9.10. Verify APU clock on (Test B)	
15.9.11. Verify SRE clock on (Test C)	
15.9.12. Verify phase is “normal” (Test D)	

	P/F	Notes
15.9.13. Execute test code “T1b.exe”.		
15.9.14. Check registers (Test A)		
15.9.15. Verify APU clock on (Test B)		
15.9.16. Verify SRE clock on (Test C)		
15.9.17. Verify phase is “normal” (Test D)		

	P/F
15.9.18. Execute test code “T1c.exe”.	
15.9.19. Check registers (Test A)	
15.9.20. Verify APU clock on (Test B)	
15.9.21. Verify SRE clock on (Test C)	
15.9.22. Verify phase is “normal” (Test D)	

15.10. Test Series T2:

(equipment setup and tests are identical to Section 15.9, except that Test D is not applicable here)

	P/F	Notes
15.10.1. Execute test code “T2.exe”.		
15.10.2. Check registers (Test A)		
15.10.3. Verify APU clock on (Test B)		
15.10.4. Verify SRE clock **OFF** (Test C)		

	P/F
15.10.5. Execute test code “T2a.exe”.	
15.10.6. Check registers (Test A)	
15.10.7. Verify APU clock on (Test B)	
15.10.8. Verify SRE clock **OFF** (Test C)	

	P/F
15.10.9. Execute test code “T2b.exe”.	
15.10.10. Check registers (Test A)	
15.10.11. Verify APU clock on (Test B)	
15.10.12. Verify SRE clock **OFF** (Test C)	

	P/F
15.10.13. Execute test code “T2c.exe”.	
15.10.14. Check registers (Test A)	
15.10.15. Verify APU clock on (Test B)	
15.10.16. Verify SRE clock **OFF** (Test C)	

15.11. Test Series T3:
(equipment setup and tests are identical to Section 15.9)

	P/F	Notes
15.11.1. Execute test code “T3.exe”.		
15.11.2. Check registers (Test A)		
15.11.3. Verify APU clock **OFF** (Test B)		
15.11.4. Verify SRE clock on (Test C)		
15.11.5. Verify phase is “normal” (Test D)		

	P/F
15.11.6. Execute test code “T3a.exe”.	
15.11.7. Check registers (Test A)	
15.11.8. Verify APU clock **OFF** (Test B)	
15.11.9. Verify SRE clock on (Test C)	
15.11.10. Verify phase is “normal” (Test D)	

	P/F
15.11.11. Execute test code “T3b.exe”.	
15.11.12. Check registers (Test A)	
15.11.13. Verify APU clock **OFF** (Test B)	
15.11.14. Verify SRE clock on (Test C)	
15.11.15. Verify phase is “normal” (Test D)	

	P/F
15.11.16. Execute test code “T3c.exe”.	
15.11.17. Check registers (Test A)	
15.11.18. Verify APU clock **OFF** (Test B)	
15.11.19. Verify SRE clock on (Test C)	
15.11.20. Verify phase is “normal” (Test D)	

15.12. Test Series T4:
(equipment setup and tests are identical to Section 15.9)

	P/F	Notes
15.12.1. Execute test code “T4.exe”.		
15.12.2. Check registers (Test A)		
15.12.3. Verify APU clock on (Test B)		
15.12.4. Verify SRE clock on (Test C)		
15.12.5. Verify phase is “**inverted**” (Test D)		

	P/F
15.12.6. Execute test code “T4a.exe”.	
15.12.7. Check registers (Test A)	
15.12.8. Verify APU clock on (Test B)	
15.12.9. Verify SRE clock on (Test C)	
15.12.10. Verify phase is “**inverted**” (Test D)	

	P/F
15.12.11. Execute test code “T4b.exe”.	
15.12.12. Check registers (Test A)	
15.12.13. Verify APU clock on (Test B)	
15.12.14. Verify SRE clock on (Test C)	
15.12.15. Verify phase is “**inverted**” (Test D)	

	P/F
15.12.16. Execute test code “T4c.exe”.	
15.12.17. Check registers (Test A)	
15.12.18. Verify APU clock on (Test B)	
15.12.19. Verify SRE clock on (Test C)	
15.12.20. Verify phase is “**inverted**” (Test D)	

16.0 Completion of Procedure:

		P/F	Notes
16.1.	Turn off power to FSU and ACU enclosures.		
16.2.	Remove PWA from enclosure per P0663 and return to storage container.		

I certify that the this procedure was performed in whole and that the data recorded above is complete and accurate.

Test Engineer _____ Date _____

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative _____ Date _____

Quality Assurance _____ Date _____