W. W. Hansen Experimental Physics Laboratory
STANFORD UNIVERSITY
STANFORD, CALIFORNIA 94305-4085

Gravity Probe B Relativity Mission

BOARD-LEVEL TEST PROCEDURE FOR THE GYROSCOPE SUSPENSION SYSTEM (GSS) FORWARD BACKPLANE (FBP) BOARD

PWA 8A01893 Rev B **S/N:** ☐

GP-B Procedure
P0601 Rev –

May 10, 2000

Prepared by: William Bencze — Date
PWA Responsible Engineer

Approved by: William Bencze — Date
RE, Gyroscope Suspension System (GSS) Group

Approved by: Dorrene Ross — Date
GP-B Quality Assurance

Table of Contents:

1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this test procedure	1-May-00	B. Bencze

2.0 Scope:

This procedure details the board-level electrical functional tests on the GSS Forward Backplane card. No mechanical or thermal stress testing shall be performed at this time.

This test plan has been written to be run with the GSS "Gold System" test fixture – an electrically and interface equivalent of the GSS flight units. In General, the Device Under Test (DUT) shall be inserted into the Gold System in place of the equivalent Gold System card, any additional electrical connections to the Gold System shall be made, and a set of software-based and possibly manual tests will be run on the board. Upon successful completion of this procedure, this board is considered electrically functional.

All data recorded during this test is recorded in this document; each test of a board will use its own copy of this procedure, and will be identified by serial number on the cover sheet.

3.0 Reference Documents

3.1. GSS Gold System Hardware and Software Configuration Standard, P0663

3.2. PWA Drawing, GSS Forward Backplane board, 8A01893

3.3. PWB Drawing, GSS Forward Backplane board, 8A01880

3.4. Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment, MIL-STD-1686

4.0 Test Facilities

HEPL Room 127, Stanford University

5.0 QA Provisions:

5.1. This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the ONR representative (E. Ingraham) shall be notified 24 hours prior to he start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

Date/time:_____	Date/time:_____
GP-B QA (D. Ross)	ONR (E. Ingraham)

5.2. Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

6.0 Test Personnel

This test procedure is to be conducted only by the following personnel:

6.1. William Bencze

6.2. Lo Van Ho

7.0 General Instructions

7.1. Redlines can be initiated by the test personnel listed in Section 6.0 and must be approved by QA.

7.2. Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.

7.3. Any nonconformance or test anomaly should be reported by a Discrepancy Report. Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.

7.4. Only the following persons have the authority to exit/terminate this test or perform a retest: Test operators listed in Section 6.0 and GP-B QA.

7.5. In this document, “Perform Flight S/W system test commands:” means to prepare the test system software as described in P0670 Board-Level Test Software Operational Procedure, and then issue the listed commands according to the procedure described in P0670.

8.0 Hardware Safety Requirements:

8.1. This assembly is ESD sensitive; special care shall be exercised per the “Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment”, MIL-STD-1686

8.2. Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

8.3. Examine all mating connectors before attempting to mate them. Remove any foreign particles. Look for any damaged pins or sockets. Do not force the coupling action if excessive resistance is encountered. Ensure that key-ways are aligned when mating connectors.

9.0 Equipment Pretest Requirements:

9.1. The GSS Gold System in which this board is to be tested must have passed successfully the P0663 – Gold System Certification Procedure prior to the start of this test. Record the Gold System serial number and date of its certification, below

Not Required

10.0 Additional Test Equipment

The following support hardware, test equipment, or software will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list may be made in the space provided.

Equipment Description	Make	Model	SN	Cal Due
1. Multimeter	Fluke			
2.				
3.				
4.				
5.				
6.				
7.				

11.0 Device Under Test (DUT):

Record the serial number of the Device Under Test, or DUT.

PWA 8A01893 GSS FBP Card	SN:	
Test Operator:	Name:	
Start of test:	Date:	

12.0 Pre-test visual inspection.

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

P/F	Test/Activity	Notes
	12.1. Remove PWA from storage container.	
	12.2. Verify that no parts are missing, unless called out in the assembly drawing.	
	12.3. Verify proper orientation of Pin 1 to PWB silkscreen on all 122 pin connectors	
	12.4. Verify the correct installation of the jumper wires as specified in the assembly drawing: JP4, JP5, JP6, JP7, JP8, JP9.	
	12.5. Verify installation of wire jumper for component FB2.	

13.0 Pre-Insertion Static Electrical Tests:

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

13.1. Power circuits isolation check

A. Set meter to "ohms", record indicated resistance between the indicated circuit points.

P/F	Test/Activity	Pass Criteria	Measurement
	13.1.1. TP8 to TP16 (M12A to AGND)	Open circuit (O.L.)	Value
	13.1.2. TP10 to TP16 (P12A to AGND)	Open circuit (O.L.)	Value
	13.1.3. TP6 to TP16 (P5A to AGND)	Open circuit (O.L.)	Value
	13.1.4. TP14 to TP16 (M50A to AGND)	Open circuit (O.L.)	Value
	13.1.5. TP15 to TP16 (P50A to AGND)	Open circuit (O.L.)	Value
	13.1.6. TP17 to TP2 (P5D to DGND)	Open circuit (O.L.)	Value
	13.1.7. TP16 to TP1 (AGND to single point ground)	< 1 ohm	Value
	13.1.8. TP2 to TP1 (DGND to single point ground)	< 1 ohm	Value

14.0 In-System Testing – Flight Configuration

Note: Tests run in this section are run with the hardware in "flight" configuration: no external test equipment or cables. The tests here use only the onboard diagnostic facilities of the GSS hardware. These will be the equivalent of the on-orbit tests of this system.

15.0 This section not applicable

15.0 In-System Testing – Ground Test Configuration

Note: Tests run in this section require the addition of test cables and external test hardware. They are used to verify the board functioning of the board in fine detail, and are only used at the time of board-level test and acceptance. These may be considered "Engineering Confidence Tests".

15.1. Test of JJ1 connector wiring:

A. Test for short circuit (< 0.1 ohm) for each of the connections noted below:
B. Connect to pins with gol-tipped Pomona test probes and test sockets.
C. Note: CN9 and CN10 are test connectors; exercise care when probing CN7; this is a flight interface

P/F	Test #	Signal	JJ1 Pin	FBP Connection	Notes
	15.1.1.	AGND	1	TP1	
	15.1.2.	P12A	2	TP10	
	15.1.3.	X_OSC	3	CN 10, Pin 107	
	15.1.4.	M12A	4	TP8	
	15.1.5.	OSC_AMP	5	CN 9, Pin 5	
	15.1.6.	HV_AMP_SEL	6	CN 9, Pin 3	
	15.1.7.	LV_AMP_SEL	7	CN 9, Pin 4	
	15.1.8.	X1_MUX_OUT	8	CN 10, Pin 111	
	15.1.9.	X2_MUX_OUT	9	CN 10, Pin 31	
	15.1.10.	X1_LV	10	*CN7, Pin 11*	
	15.1.11.	X2_LV	11	*CN7, Pin 92*	
	15.1.12.	X_TEMP_MON	12	CN 10, Pin 121	
	15.1.13.	X1_HV_MON	13	CN 10, Pin 119	
	15.1.14.	X2_HV_MON	14	CN 10, Pin 39	
	15.1.15.	-	15	(NONE)	
	15.1.16.	X_POS	16	CN 9, Pin 103	
	15.1.17.	-	17	(NONE)	
	15.1.18.	P12A	18	TP10	
	15.1.19.	-	19	(NONE)	
	15.1.20.	M12A	20	TP8	

15.2. Test of JJ2 connector wiring:

A. Test for short circuit (< 0.1 ohm) for each of the connections noted below:
B. Connect to pins with gold-tipped Pomona test probes and test sockets.
C. Note: CN9 and CN10 are test connectors; *exercise care when probing CN7; this is a flight interface*

P/F	Test #	Signal	JJ1 Pin	FBP Connection	Notes
	15.2.1.	AGND	1	TP1	
	15.2.2.	P12A	2	TP10	
	15.2.3.	Y_OSC	3	CN 10, Pin 28	
	15.2.4.	M12A	4	TP8	
	15.2.5.	OSC_AMP	5	CN 9, Pin 5	
	15.2.6.	HV_AMP_SEL	6	CN 9, Pin 3	
	15.2.7.	LV_AMP_SEL	7	CN 9, Pin 4	
	15.2.8.	Y1_MUX_OUT	8	CN 10, Pin 72	
	15.2.9.	Y2_MUX_OUT	9	CN 10, Pin 112	
	15.2.10.	Y1_LV	10	*CN7, Pin 13*	
	15.2.11.	Y2_LV	11	*CN7, Pin 94*	
	15.2.12.	Y_TEMP_MON	12	CN 10, Pin 41	
	15.2.13.	Y1_HV_MON	13	CN 10, Pin 80	
	15.2.14.	Y2_HV_MON	14	CN 10, Pin 120	
	15.2.15.	-	15	(NONE)	
	15.2.16.	Y_POS	16	CN 9, Pin 23	
	15.2.17.	-	17	(NONE)	
	15.2.18.	P12A	18	TP10	
	15.2.19.	-	19	(NONE)	
	15.2.20.	M12A	20	TP8	

15.3. Test of JJ3 connector wiring:

A. Test for short circuit (< 0.1 ohm) for each of the connections noted below:
B. Connect to pins with gol-tipped Pomona test probes and test sockets.
C. Note: CN9 and CN10 are test connectors; *exercise care when probing CN7; this is a flight interface*

P/F	Test #	Signal	JJ1 Pin	FBP Connection	Notes
	15.3.1.	AGND	1	TP1	
	15.3.2.	P12A	2	TP10	
	15.3.3.	Z_OSC	3	CN 10, Pin 69	
	15.3.4.	M12A	4	TP8	
	15.3.5.	OSC_AMP	5	CN 9, Pin 5	
	15.3.6.	HV_AMP_SEL	6	CN 9, Pin 3	
	15.3.7.	LV_AMP_SEL	7	CN 9, Pin 4	
	15.3.8.	Z1_MUX_OUT	8	CN 10, Pin 32	
	15.3.9.	Z2_MUX_OUT	9	CN 10, Pin 73	
	15.3.10.	Z1_LV	10	*CN7, Pin 15*	
	15.3.11.	Z2_LV	11	*CN7, Pin 96*	
	15.3.12.	Z_TEMP_MON	12	CN 10, Pin 122	
	15.3.13.	Z1_HV_MON	13	CN 10, Pin 40	
	15.3.14.	Z2_HV_MON	14	CN 10, Pin 81	
	15.3.15.	-	15	(NONE)	
	15.3.16.	Z_POS	16	CN 9, Pin 64	
	15.3.17.	-	17	(NONE)	
	15.3.18.	P12A	18	TP10	
	15.3.19.	-	19	(NONE)	
	15.3.20.	M12A	20	TP8	

16.0 Completion of procedure:

P/F	Test/Activity	Notes
	16.1. Return PWA to storage container	

I certify that the this procedure was performed in whole and that the data recorded above is complete and accurate.

Test Engineer		Date	

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative		Date	
Quality Assurance		Date	