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Gravity Probe B Relativity Mission

BOARD-LEVEL TEST PROCEDURE FOR THE GYROSCOPE SUSPENSION SYSTEM (GSS) FSU FORWARD MODE REGISTER (FMR) BOARD

PWA 8A01892 Rev F **S/N:** ☐

GP-B Procedure
P0602 Rev C
September 24, 2001

Prepared by: Scott Smader — Date
RE, FMR

Approved by: William Bencze — Date
RE, Gyroscope Suspension System (GSS) Group

Approved by: Dorrene Ross — Date
GP-B Quality Assurance

Table of Contents:

1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this test procedure	29-Feb-00	S Smader
A0	Clarify software command usage	4-Apr-00	S Smader
A1	Typos	6-Apr-00	S Smader
A	Second release	7-Apr-00	S Smader
B	Add 12.9; 15.0. Board Rev E. PONRST test	20-Oct-00	S Smader
C	Per ECO 1307: invert HBEAT_OK	24-Sep-01	S Smader

2.0 Scope:

This procedure details the board-level electrical functional tests on the GSS Forward Mode Register (FMR) card. No mechanical or thermal stress testing shall be performed at this time.

This test plan has been written to be run with the GSS "Gold System" test fixture – an electrically and interface equivalent of the GSS flight units. In General, the Device Under Test (DUT) shall be inserted into the Gold System in place of the equivalent Gold System card, any additional electrical connections to the Gold System shall be made, and a set of software-based and possibly manual tests will be run on the board. Upon successful completion of this procedure, this board is considered electrically functional.

All data recorded during this test is recorded in this document; each test of a board will use its own copy of this procedure, and will be identified by serial number in the upper right corner.

3.0 Reference Documents

3.1. GSS Gold System Hardware and Software Configuration Standard, P0663

3.2. PWA Drawing, GSS Forward Mode Register board, 8A01892

3.3. PWB Drawing, GSS Forward Mode Register board, 8A01877

3.4. Programming specification, GSS FCL PAL, PN: 26221 Rev-

3.5. Board-level test software operational procedure, P0670

3.6. Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment, MIL-STD-1686

4.0 Test Facilities

HEPL Room 127, Stanford University

5.0 QA Provisions:

5.1. This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the ONR representative (E. Ingraham) shall be notified 24 hours prior to he start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

Date/time:_____ Date/time:_____

GP-B QA (D. Ross) ONR (E. Ingraham)

5.2. Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

6.0 Test Personnel

This test procedure is to be conducted only by the following certified personnel:

6.1. William Bencze

6.2. Scott Smader

6.3. Joe Kilner

6.4. Lo Van Ho

7.0 General Instructions

7.1. Redlines can be initiated by the certified test personnel listed in Section 6.0 and must be approved by QA.

7.2. Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.

7.3. Any nonconformance or test anomaly should be reported by a Discrepancy Report. Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.

7.4. Only the following persons have the authority to exit/terminate this test or perform a retest: Certified test operators listed in Section 6.0 and GP-B QA.

7.5. In this document, “Perform Flight S/W system test commands:” means to prepare the test system software as described in P0670 Board-Level Test Software Operational Procedure, and then issue the listed commands according to the procedure described in P0670.

8.0 Hardware Safety Requirements:

8.1. This assembly is ESD sensitive; special care shall be exercised per the “Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment”, MIL-STD-1686

8.2. Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

8.3. Examine all mating connectors before attempting to mate them. Remove any foreign particles. Look for any damaged pins or sockets. Do not force the coupling action if excessive resistance is encountered. Ensure that key-ways are aligned when mating connectors.

Board S/N:

9.0 Equipment Pretest Requirements:

9.1. The GSS Gold System in which this board is to be tested must have passed successfully the P0663 – Gold System Certification Procedure prior to the start of this test. Record the Gold System serial number and date of its certification, below

GSS Gold System	SN:	
	Date of Certification	
	Configuration (circle one)	Full Partial

10.0 Additional Test Equipment

The following support hardware, test equipment, or software will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list may be made in the space provided.

Equipment Description	Make	Model	SN	Cal Due
1. Multimeter	Fluke			
2.				
3.				
4.				

11.0 Device Under Test (DUT):

Record the serial number of the Device Under Test, or DUT.

PWA 8A01892 Rev F GSS Forward Mode Register	SN:	

Test Operator:	Name:	

Start of test:	Date:	

Board S/N:

12.0 Pre-test visual inspection.

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

		P/F	Notes
12.1.	Remove PWA from storage container.		
12.2.	Verify that no parts are missing, unless called out in the assembly drawing.		
12.3.	Verify that the following capacitors are installed in the proper orientation: C1, C90, C91, C103, C104.		
12.4.	Verify that pin 1 of the resistor packs are installed in the square pad hole or adjacent to the silkscreened triangle on the PWB: RP1-6, RS1-10.		
12.5.	Verify the correct installation of jumper wires as specified in the assembly drawing: PWA Notes 25, 26.		
12.6.	Verify the proper orientation of pin 1 of all DIP packages: U1 through U35.		
12.7.	Verify that diodes have been installed with correct orientation: D1-64		
12.8.	Verify the part number(s) of the following programmable device(s) match(es) the PN on the latest release of the assy drawing bill of materials for this card: U29		
12.9.	Verify rework per assembly drawing: PWA, Note 29.		

Board S/N:

13.0 Pre-Insertion Static Electrical Tests:

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

13.1. Power circuits isolation check

A. Set meter to "ohms", record indicated resistance between the indicated pins.

B. Check for open or closed circuit between each two points.

DUT passes this section if all measurements are high impedance, > 2 kohms.

	P/F	Measurement
13.1.1. P1-28 to P1-122 (P5D to DGND)		
13.1.2. P1-1 to P1-28 (MR_12V to P5D)		
13.1.3. P1-1 to P1-122 (MR_12V to DGND)		
13.1.4. P1-1 to P1-2 (MR_12V to MR_RET)		
13.1.5. P1-2 to P1-28 (MR_RET to P5D)		
13.1.6. P1-16 to P1-28 (GND_CHASSIS to P5D)		
13.1.7. P1-16 to P1-1 (GND_CHASSIS to MR_12V)		

Note: MR_RET may be shorted to DGND and/or GND_CHASSIS, but these conditions are not part of this board's qualification procedure.

14.0 In-System Testing – Flight Configuration

Note: Tests run in this section are run with the hardware in "flight" configuration: no external test equipment or cables. The tests here use only the onboard diagnostic facilities of the GSS hardware. These will be the equivalent of the on-orbit tests of this system.

Except at the discretion of the test director, these tests shall not be run before all Pre-Insertion Static Electrical Tests and all In-System Ground Configuration Tests have successfully completed.

14.1. Board installation:

		P/F	Notes
14.1.1.	Install PWA in gold system enclosure per the instructions in P0663 – Gold System certification procedure		
14.1.2.	Cable system for "Configuration B" per P0663 – Gold System certification procedure *(RAD6000)*		

14.2. System Tests:

Record the Pass/Fail return status of each of the following commands.

		P/F	
14.2.1.	Perform Flight S/W system test commands: 14 1 14 29 If this completes successfully, record Pass for this test. Otherwise record 'Fail'.		

DUT passes this section if all of the return values are Pass.

15.0 In-System Testing – Ground Test Configuration

Note: Tests run in this section require the addition of test cables and external test hardware. They are used to verify the board functioning of the board in fine detail, and are only used at the time of board-level test and acceptance. These may be considered "Engineering Confidence Tests".

15.1. Power On Reset Test

(Continues on next page.)

	P/F	Notes
15.1.1. Connect jumper JP32 pins 1 and 2.		
15.1.2. Perform Flight S/W system test commands: 16 100 16 3 0 16 3 1 16 3 2 16 3 3 16 3 4 16 3 5 16 3 6 16 3 7 16 3 8 16 3 9 16 3 10 16 3 11 16 3 12 16 3 13 16 3 14 16 3 15 On PC610, confirm that LEDs D25-D40 are lit.		LED D32 status does not affect Pass/Fail Result.
15.1.3. On PC610, move jumper JP32 to pins 2 and 3. Confirm that LEDs D25-D40 are extinguished.		LED D32 status does not affect Pass/Fail Result.
15.1.4. On PC 610, move jumper between JP32 pins 1 and 2. Confirm that LEDs D25-D31 and D33-D40 remain extinguished.		LED D32 status does not affect Pass/Fail Result.
15.1.5. Perform Flight S/W system test commands: 16 3 8 On PC610, confirm that LEDs D25-D40 are lit.		LED D32 status does not affect Pass/Fail Result.

16.0 HBEAT_OK Test:

	P/F	Notes
16.1. Perform Flight S/W system test commands: 1 7 16 100 16 5 1 16 1 0x28c Confirm that the most significant bit of Monitor 3 is 0.		MSB of Monitor 3 is the HBEAT_OK status. 0=OK; 1=Error. Same information is available in PitView's Timing and Status Info window as "HBEAT_OK".
16.2. Using a multimeter, confirm that PC610 J3-11 is logic low relative to DGND.		
16.3. Perform Flight S/W system test commands: 1 6 16 1 0x28c Confirm that the most significant bit of Monitor 3 is 1.		
16.4. Using a multimeter, confirm that PC610 J3-11 is logic high relative to DGND.		

Board S/N:

17.0 Completion of procedure:

		P/F	Notes
17.1.	Turn off power to FSU and ACU enclosures.		
17.2.	Remove PWA from enclosure per P0663 and return to storage container.		

I certify that this procedure was performed in whole and that the data recorded above is complete and accurate.

Test Engineer _____ Date _____

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative _____ Date _____

Quality Assurance _____ Date _____