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Gravity Probe B Relativity Mission

BOARD-LEVEL TUNING PROCEDURE FOR THE GYROSCOPE SUSPENSION SYSTEM (GSS) AFT CLOCK SUPPORT (ACS) BOARD

PWA 8A01898 Rev D **S/N:**

GP-B Procedure
P0666 Rev B

Prepared by: Joseph R. Kilner Date

Approved by: William J. Bencze Date
RE, Gyroscope Suspension System (GSS) Group

Approved by: Dorrene Ross Date
GP-B Quality Assurance

Board S/N:

Table of Contents:

1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this procedure	10-MAR-00	JR Kilner
A	Modified based on dry-runs performed on gold system cards	27-Mar-00	JR Kilner
B	Corrected error in parts lists in Appendix A per ECO 11129	24-Apr-00	WJ Bencze

2.0 Scope:

This procedure details the operations required to tune the phase locked loop (PLL) on this board. This tuning is required before formal testing of the card can begin. No mechanical or thermal stress testing shall be performed at this time.

This procedure has been written to be run with the GSS "Gold System" test fixture – an electrically and interface equivalent of the GSS flight units. In General, the board under test shall be inserted into the gold system in place of the equivalent gold system card, any additional electrical connections to the gold system shall be made, and a set of software-based and possibly manual tests will be run on the board. Upon successful completion of this procedure, this board is considered electrically functional.

All data recorded during this test is recorded in this document; each test of a board will use its own copy of this procedure, and will be identified by serial number in the upper right corner.

3.0 Reference Documents

3.1. GSS Gold System Hardware and Software Configuration Standard, S0663

3.2. PWA Drawing, GSS Aft Clock Support board, 8A01898

3.3. PWB Drawing, GSS Aft Clock Support board, 8A01874

3.4. Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment, MIL-STD-1686

4.0 Test Facilities

HEPL Room 127, Stanford University.

5.0 QA Provisions:

5.1. This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the ONR representative (E. Ingraham) shall be notified 24 hours prior to he start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

Date/time:_____	Date/time:_____
GP-B QA (D. Ross)	ONR (E. Ingraham)

5.2. Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

6.0 Test Personnel

This test procedure is to be conducted only by the following certified personnel:

6.1. William Bencze

6.2. Scott Smader

6.3. Joe Kilner

6.4. Lo Van Ho

7.0 General Instructions

7.1. Redlines can be initiated by the certified test personnel listed in Section 6.0 and must be approved by QA.

7.2. Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.

7.3. Any nonconformance or test anomaly should be reported by a Discrepancy Report. Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.

7.4. Only the following persons have the authority to exit/terminate this test or perform a retest: Certified test operators listed in Section 6.0 and GP-B QA.

8.0 Hardware Safety Requirements:

8.1. This assembly is ESD sensitive; special care shall be exercised per the “Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment”, MIL-STD-1686

8.2. Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

8.3. Examine all mating connectors before attempting to mate them. Remove any foreign particles. Look for any damaged pins or sockets. Do not force the coupling action if excessive resistance is encountered. Ensure that key-ways are aligned when mating connectors.

9.0 Equipment Pretest Requirements:

9.1. The GSS Gold System in which this board is to be tested must have passed successfully the P0663 – Gold System Certification Procedure prior to the start of this test. Record the Gold System serial number and date of its certification, below

GSS Gold System	SN:	
	Date of Certification	
	Configuration (circle one)	Full Partial

Board S/N:

10.0 Test Equipment

The following support hardware, test equipment, or software will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list may be made in the spaces provided.

Equipment Description	Make	Model	SN	Cal Due
1. GSS Gold System (partial or full)				
2. Digital Multimeter	Fluke			
3. Digital Oscilloscope with probes	Tektronix			
4. Analog Oscilloscope with probes	Tektronix			
5. PC with PC-EBI interface card and cable	-	-		NR
6. SRE Clock simulator	-	-		NR
7. Programmable clock generator	Stanford Research Systems (SRS)			
8. PC355 Test card				NR
9.				
10.				

11.0 Device Under Test (DUT):

Record the serial number of the board under test (ie, Device Under Test, or DUT).

PWA 8A01898C GSS Aft Clock Support	SN:	
Test Operator:	Name:	
Start of test:	Date: Time:	

Board S/N:

12.0 Pre-test visual inspection.

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected a an ESD certified station. Wrist straps and/or heel grounding straps shall be used. An ESD approved laboratory coat shall be worn when in close proximity to this PWA.

		P/F	Notes
12.1.	Remove PWA from storage container.		
12.2.	Verify that no parts are missing, unless called out in the assembly drawing.		
12.3.	Verify the proper orientation of pin 1 of all DIP packages: All DIPs have pin 1 farthest from the 120-pin connector.		
12.4.	Verify that D1, D2, and D3 have been installed with the correct orientation.		
12.5.	Verify that Q1 is installed with the correct orientation.		
12.6.	Verify that a temporary C13 capacitor is installed on test leads in the range of 10 pF to 27 pF Record value at the right.		Value of C13:

Board S/N:

13.0 Pre-Insertion Static Electrical Tests:

Note: All handling of this PWA shall be performed using ESD control methods, as outlined MIL-STD-1686. Unit shall be inspected a an ESD certified station. Wrist straps and/or heel grounding straps shall be used. An ESD approved laboratory coat shall be worn when in close proximity to this PWA.

13.1. Power circuit isolation check

Set meter to "ohms", record indicated resistance between the indicated pins. Note the polarity for meter hookup.

Pass/Fail criterion: DUT passes if all resistance measurements are > 100 kohms.

	P/F	Notes
13.1.1. (+) to P2 pin 120 [Vcc] ↔ (-) to P2 pin 2 [AGND]		Measurement: Ohms.
13.1.2. (+) to P2 pin 1 [P15V] ↔ (-) to P2 pin 118 [DGND]		Measurement: Ohms.
13.1.3. (+) to P2 pin 118 [DGND] ↔(-) to P2 pin 3 [M15V]		Measurement: Ohms.

14.0 Test Equipment Setup

14.1. Board installation:

		P/F	Notes
14.1.1.	Install PWA in gold system enclosure per the instructions in P0663 – Gold System certification procedure		
14.1.2.	Cable system for “Configuration A” per P0663 – Gold System certification procedure (PC-EBI)		

14.2. Test Equipment Setup.

		P/F
14.2.1.	Connect the Function Generator output (Function output) to the Ext 16f_0 A input of the Clock Emulator.	
14.2.2.	Connect the 16f_0 A output of the Clock Emulator to channel 1 of the digital oscilloscope through a co-ax.	
14.2.3.	Connect the FPGA_DIAG monitor (pin 21 of the 25-pin connector on the Test Fixture) to channel 2 of the digital oscilloscope using a 10:1 probe. (Connect all of the probe grounds to pin 13.)	
14.2.4.	Connect the APU clock (via BNC on Aft power supply module) to channel 3 of the digital oscilloscope using a 10:1 probe.	
14.2.5.	Connect INT0 (pin 25 of the 25-pin connector on the Test Fixture) to channel 4 of the digital oscilloscope using a 10:1 probe.	
14.2.6.	Connect INT1 (BNC connector on the Test Fixture) to channel 1 of the analog oscilloscope.	
14.2.7.	Connect INT2 (BNC connector on the Test Fixture) to channel 2 of the analog oscilloscope.	
14.2.8.	Connect INT3 (pin 11 of the 25-pin connector on the Test fixture) to channel 3 of the analog oscilloscope.	

	P/F	Notes
14.2.9. Function Generator settings: A. Select square wave, B. frequency = 16.368000 MHz, C. Ampl = 4.60V, D. Offset = 2.50V, E. leave display on 'frequency' with step size = 100.		
14.2.10. GSS-SRE Clock Emulator switch settings: A. ON; 10Hz A, 16fo A, Ext 16fo. B. OFF; 10Hz B, 16fo B, Ext 10Hz.		

14.3. Digital Scope Setup:

	P/F
14.3.1. Vertical Menu: Position; place channel one at the top followed by channels two, three, and four; Scale; set to 5V per cm (may indicate 500mV per cm if scope does recognize the probe as a 10:1 probe); set all channels to full bandwidth and DC coupling	
14.3.2. Horizontal Menu: Select Main Time Base, set Trigger Position = 50%, Set Record Length = 1000, (if available on scope) set Fit-to-screen = OFF (in Extd Acq Setup)	
14.3.3. Trig Menu: Type = edge, Source = Channel 4, Coupling = DC, Slope = rising, Level = about half of max (250mV), set to Auto Trig, set Holdoff = minimum	
14.3.4. Acquire Menu: Mode = Hi Res, Repetitive Signal = OFF (or ON for a lower sampling frequency scope), Stop After = R/S button, Limit test = OFF	
14.3.5. Measure the frequencies of channels one, two, and three – setup these measurements in this order	
14.3.6. When running, press the "Clear Menu" button to achieve an uncluttered display	
14.3.7. Use a sweep speed of 100 nsec per cm or slower depending on the signal of interest	

14.4. Test Software

Notes on the test software display:

The top line of the display contains a 16-bit (4 Hex characters) counter incrementing at about 20 counts per second whenever the program is running. Following two lines of labels, the next line displays the data that the program is writing to registers 0, 1, 4, and 5 on the AMT board. The next line lists the data read back from the same four registers plus five status bits read from the PC_EBI board.

Except for the status bits that are displayed in binary, all displays are 16-bit words displayed in Hex. In Hex, 4 bits (representing the decimal values from 0 to 15) are displayed as 0 … 9, a, b, c, d, e, f where a = 10, f = 15, etc. The right character of the Hex word is formed from the four LS bits (3, 2, 1, and 0); the next Hex character is formed from bits 7, 6, 5, and 4; etc.

The read-back data should be the same as the written data except as follows:

A. *If the right two nibbles of Reg 0 consist of only 0's and/or 7's, 0080 is added to the Reg 0 read back;*
B. *The MS bit of Reg 1 is INT4 (this is the internally generated equivalent of INT0);*
C. *The two bits represented by 8800 in Reg 4 are the latched and unlatched readings of the AMT diagnostic Mux whenever it is enabled;*
D. *The right byte of Reg 5 is read back in the left byte; and the right nibble of Reg 5 is the input-only PPin (bit 7 is the ADC latchup flag.*

The status bits are latched on the PC_EBI board as they occur. The status, flag, and INT4 bits are cleared under program control just after they are read. It is normal for the DACK status bit to remain at zero.

Next shown are the 16 A-to-D converter readings along with their labels.

The last line of the display lists the test number and a short description of the test.

Board S/N: _____

15.0 PLL Tuning operations

The purpose of this procedure is to determine the best value of the capacitor to use for C13. Choose C13 from the following six values: 10pf, 12pf, 15pf, 18pf, 22pf, or 27pf. Use a 15pf capacitor for the first try. For subsequent boards, use the final value from the previous board.

The PLL is locked when the input clock (nominally 16.368000 MHz) remains synchronized with the other clocks that are displayed on the digital oscilloscope. In addition, the "PLL Control Effort" (nominal range, in hex = 0000 to 7FFF) is to remain at least 40 (hex) inside the extreme limits. These limits are easily determined by setting the input clock frequency slightly above and slightly below the lock range.

Perform the following steps to test and tune the PLL operation:

1. Tack solder the trial capacitor to the wires installed in place of C13. Use short leads (less than about 1 cm.) for the installed wires and the test capacitor. Record the value of C13 on the following data sheet. (make additional copies of this sheet as needed)
2. Install the ACS board in the Gold System and plug-in the clock cable per the installation procedure in P0633, Gold System Configuration Procedure.
3. Turn on the power.
4. Start ACS test program.
5. Measure and record the highest frequency at which the PLL remains locked (PLL control effort < 7ffff).
6. Measure and record the PLL control effort at 16.368000 MHz.
7. Measure and record the lowest frequency at which the PLL remains locked (Pll control effort > 0).
8. Remove the ACS board per the installation procedure in P0633, Gold System Configuration Procedure.
9. Evaluate the success criteria for this test capacitor.
10. If this capacitor gives acceptable performance, record the value below; if not, repeat steps 1-9 for a new capacitor value. Use a smaller capacitor to raise the central frequency and a larger capacitor to lower it.

Success criteria: An acceptable value for C13 permits the Phase-Locked-Loop to remain locked for input clock frequencies in the range 16.368MHz +/- 500Hz. If possible, the center of the lock range should be 16.368MHz +/- 100Hz. When measuring the lock range and central frequency, vary the input clock by steps of +/- 100Hz.

Acceptable value of C13: _____ pF

Record this value in the "Select and Test Component Installation Instruction Sheet" and (at the end of this procedure) and attach the sheet to the traveler for this PWA.

Board S/N:

Test data sheets for trial values of C13. Make additional copies of this sheet as necessary.

Test Value of C13: __________	Notes
1. Slew the frequency generator up from 16.368000 MHz and record the frequency where the PLL loses lock.	High lock frequency
2. Set frequency generator to 16.368000 MHz; verify PLL remains locked. Record PLL control effort	PLL ctrl effort.
3. Slew the frequency generator down from 16.368000 MHz and record the frequency where the PLL loses lock.	Low lock frequency

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2. Set frequency generator to 16.368000 MHz; verify PLL remains locked. Record PLL control effort	PLL ctrl effort.
3. Slew the frequency generator down from 16.368000 MHz and record the frequency where the PLL loses lock.	Low lock frequency

Board S/N:

16.0 Completion of Procedure:

		P/F	Notes
16.1.	Remove PWA from enclosure per P0663 and return to storage container.		
16.2.	Attach a copy of the “Select-and-test Installation Instructions” sheet to the board traveler.		
16.3.	Return the board to the assembly vendor for installation of final value of C13.		

The results obtained in the performance of this test procedure are acceptable.

Test Engineer _____ Date _____

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative _____ Date _____

Quality Assurance _____ Date _____

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Gravity Probe B Relativity Mission

P0666B APPENDIX A
SELECT AND TEST COMPONENT
INSTALLATION INSTRUCTION SHEET
GSS ACS PWA

PWA 8A01898 Rev D S/N: ____

From the findings of procedure P0666, "BOARD-LEVEL TUNING PROCEDURE FOR THE GYROSCOPE SUSPENSION SYSTEM (GSS) AFT CLOCK SUPPORT (ACS) BOARD", install the following select-and-test components as indicated below:

Install for C13 (check one)	Flight PN	Description
	CMR03C10R0DOCR	Capacitor, 10pF, Mica
	CMR03C12R0DOCR	Capacitor, 12pF, Mica
	CMR03C150DOCR	Capacitor, 15pF, Mica
	CMR03C180DOCR	Capacitor, 18pF, Mica
	CMR03E220DOCR	Capacitor, 22pF, Mica
	CMR03E270DOCR	Capacitor, 27pF, Mica

Approved:

GSS Representative ____ Date ____

Quality Assurance ____ Date ____