GRAVITY PROBE B

PROCEDURE FOR

PAYLOAD VERIFICATION

(PTP) TRE Software Checkout Procedure

P0822 Rev. -

June 11, 2001

Prepared by: Bob Farley

Approvals:

Program Responsibility	Signature	Date
Bob Farley TRE REE		
Bill Bencze Payload Test Director		
Richard Whelan GP-B System Engineering		
D. Ross GP-B Quality Assurance		
Rob Brumley GP-B Payload Technical Manager		

NOTES:

Level of QA required during performance of this procedure:

_4_ Stanford QA Representative

All redlines must be approved by QA

Revision Record:

Rev	Rev Date	ECO #	Summary Description
-	June 11, 2001	NA	Original issue

Acronyms and Abbreviations:

Acronym / Abbreviation	**Meaning**
DMA	Detector Mount Assembly
GSE	Ground Support Equipment
TRE	Telescope Readout Electronics
AS3	Artificial Star #3

Table of Contents

1. Scope

This procedure uses the flight TREs connected to the flight SREs and SRE Test set to command the TREs and verify the functioning of associated software modules. It is likely that this procedure might be conducted with less than a full complement of TREs and SREs. As a minimum, one Forward SRE and one Aft SRE and one SRE Test set are required to conduct this procedure.

This procedure ☐ Does ☒ Does not	provide formal verification of GP-B trquirements.
This procedure ☐ Does ☒ Does not	include constraints and restrictions for the Payload.

2. Safety Requirements

2.1 Potential Hazards

2.1.1 The electronic systems are subject to damage by electrostatic discharge.

2.1.2 Connectors are subject to wear or damage during mating.

2.2 Mitigation of hazards

2.2.1 Connection and disconnection shall be performed only when the equipment involved is in a powered-down state.

2.2.2 Connector savers are to be used on the TRE and tophat connectors.

Note: The mating and demating of all flight connectors must be recorded in a log. This procedure does not require removal or replacement of connector savers onto the flight connectors--they should already be in place.

2.2.3 Connectors shall be inspected for contamination and for bent, damaged, or recessed pins prior to mating.

2.2.4 Grounded wrist straps are to be worn prior to removal of connector caps or covers and during mating/demating operations.

2.2.5 ESD-protective caps or covers are to be immediately installed after demating of connectors.

2.3 Injuries

3. Quality Assurance

3.1 QA Notification

QA to notify ONR 24 hours prior to beginning of testing.

Person Contacted: _____ Date and Time: _____

3.2 Red-line Authority

Authority to red-line (make minor changes during execution) this procedure is given solely to the PTD or his designate and shall be approved by the QA Representative. Additionally, approval by the Hardware Manager shall be required if, in the judgment of the PTD or QA Representative, experiment functionality may be affected.

3.3 Discrepancies

Testing shall be conducted on a formal basis to approved and released procedures. The QA program office shall be notified of the start of this procedure. A Quality Assurance Representative, designated by D. Ross shall be present during the procedure and shall review any discrepancies noted and approve their disposition. Upon completion of this procedure, the QA Program Engineer, D. Ross or her designate, will certify concurrence that the effort was performed and accomplished in accordance with the prescribed instructions by signing and dating in the designated place(s) in this document. Discrepancies will be recorded in a D-log or as a DR per Quality Plan P0108.

4. Test Personnel

4.1 Personnel Requirements

4.1.1 A test set operator familiar with executing CSTOL procedures is required for this procedure:

4.1.2 This test is to be conducted under the direction of certified technical personnel.

4.1.3 This procedure collects performance data on the science slope algorithm and the PID temperature control algorithm that must be analyzed to determine whether parameter changes are needed.

4.2 Qualified Personnel

4.2.1 Operators

Werner Growitz, Scott Jankowski, Paul Mcgown, and Thomas Wai

4.2.2 Test conductors

John Goebel, Bob Farley.

4.2.3 Data analysts

Peter Boretsky

5. Requirements

5.1 Hardware Required

5.1.1 Commercial test equipment

Manufacturer	Model	Serial Number	Calibr. Exp. Date
SUN Workstation (Test Set)	Ultra 1 3D Creator		

5.1.2 Mechanical/Electrical Special test equipment

Description	Part No.	Rev. no.	Serial No.	Certification Date

5.1.3 Tools

5.1.4 Custom

Description	Model number	No. Req'd
Octolite--Telescope Near Field Stimulator	8A02659GSE	1
Flight Cable, TRE-A to Tophat connector I9	8A01288-101	1
Flight Cable, TRE-B to Tophat connector I8	8A01287-101	1
Flight Power cable W458	8A01412	2
Flight Digital cable W459	8A01413	2
Flight Analog 1 cable W456, modified per 8A01410, Rev. A	8A01410	2
Flight Analog 2 cable W457, modified per 8A01411, Rev. A	8A01411	2
Forward SRE A	P/N 8A00848-101	1
Forward SRE B	P/N 8A00848-102	1
Aft SRE	P/N 8A00920-101 or -102	1
SRE Test Set		1
Aft SRE A, Fwd SRE A Power W400 Cable Assembly	8A00557-101 Rev. -	1
Aft SRE A, Fwd SRE A Digital W401 Cable Assembly	8A00558-101 Rev.	1
Aft SRE B, Fwd SRE A Power W402 Cable Assembly	8A00559-101 Rev.	1
Aft SRE B, Fwd SRE A Digital W403 Cable Assembly	8A00560-101 Rev.	1
SRE A, HLD's W404 Cable Assembly	8A00561-101 Rev.	1
Aft SRE A, Fwd SRE B Digital W405 Cable Assembly	8A00562-101 Rev.	1
Aft SRE A, Fwd SRE B Power W406 Cable Assembly	8A00563-101 Rev.	1
Aft SRE B, Fwd SRE B Digital W407 Cable Assembly	8A00564-101 Rev.	1
Aft SRE B, Fwd SRE B Power W408 Cable Assembly	8A00565-101 Rev.	1
SRE B, HLD's W409 Cable Assembly	8A00566-101 Rev.	1
SRE A Htr Pwr W410 Cable Assembly	8A00567-101 Rev. A	1
SRE B Htr Pwr W411 Cable Assembly	8A00568-101 Rev. A	1
Wiring Diagram, FWD SRE J3 to Top Hat W412 & W413	8A01317-101 Rev. A	1
SRE to ACU Timing W414 Cable Assembly	8A01484-101 Rev. -	1
SRE to ECU Timing W415 Cable Assembly	8A01485-101 Rev. -	1
SRE Spacecraft Emulator GSE	Certified using P0843 Rev-	1

5.2 Software Required

5.2.1 Flight Software

Flight Software Name	Version No.
MSS (Mission Support Software)	3.0.4S

5.2.2 CSTOL Scripts

CSTOL Script Name		Version No.
plv2trei.prc	Payload Verification 2 TRE Master Proc	
adjust_clamps.prc		
adjust_dtemp.prc		
sta_negxgain.prc		
sta_negygain.prc		
sta_posxgain.prc		
sta_posygain.prc		
stb_negxgain.prc		
stb_negygain.prc		
stb_posxgain.prc		
stb_posygain.prc		
tre_clmpmon_br.prc		
tre_det_a_bal_br.prc		
tre_det_b_bal_br.prc		
tre_detbal_br.prc		
tre_heat_br.prc		
tre_hilov_br.prc		
tre_pwr_br.prc		
tre_ref_br.prc		
tre_scislp_br.prc		
tre_tsrvo_br.prc		
unit_swap.prc		

5.2.3 SPC Scripts

SPC Script Name	Version No.
N/A	

5.2.4 Test Support Software

Test Software Name	Version No.
Oasis (Operating System Software)	V 2.4.5
Framex (front end software)	framexs

5.3 Procedures or Op Orders Required

Procedure Name	Procedure No.
(PTP) Procedure for TRE Detector Stimulus Test	P0753 Rev. B
Procedure for TRE Aliveness Test Following Payload Insertion	P0487
Procedure for TRE / DMA Temperature Control Verification	P0488
Procedure for TRE Nominal Function Test	P0489
SRE_TestSet_RS232Operations_1.2	
SQUID Readout Electronics (SRE) Usage in Payload Test II	P0833 Rev -

5.4 References and Applicable Documents

Description	
SRE_TestSet_RS232Operations_1.2	
SRE testset VDC (version description document)	LMMS # P480213C

5.5 Equipment Pretest Requirements

Procedure P0489, *(PTP) Procedure for TRE Nominal Function Test,* shall have been completed prior to this procedure.

5.6 Configuration Requirements

5.6.1 Probe is installed in the dewar. Probe pressure <1E-5 torr. TRE mounted on dewar, with cables connected to tophat. Flight Forward SREs are mounted to the TREs and connected thereto with flight cables. The Forward SREs are connected to one or more AFT SRE and thence to a dedicated test set.

5.6.2 Dewar and probe are cooled with liquid helium.

5.6.3 Artificial Star #3 (AS3) installed on probe (likely, but not required).

5.6.4 If AS3 is not installed, then a transparent cover must be installed to protect window #4, and aluminum foil available to optionally block extraneous light.

5.6.5 The Forward and Aft SREs shall have been connected to the test set, and operated with one or more procedure prior to initiation of this procedure. SRE_TestSet_RS232Operations_1.2 shall have been completed prior to start of this procedure.

5.6.6 The flight cables between the forward SRE and the TRE units shall have been installed prior to initiation of this procedure.

5.6.7 The TREs shall have been connected to the tophat I8 and I9 connectors prior to the initiation of this procedure.

5.7 Verification / Success Criteria

This procedure uses software that has not been previously tested with a fully functional environment. The balance algorithm and the PID temperature control have never been tested with the detector modules that provide the inputs and receive the stimulii supplied by the software; the test is to determine if the algorithms act as expected. The engineering data filter algorithm has been tested in the ITF (integrated test facility) and should provide realistic values when used in conjunction with the calibrations.

The success criteria are to complete the procedure, exercising all of the applicable algorithms, and recording bridge files. Offline, later analysis of the bridge file data will provide inputs for the data reduction capability.
It is likely that portions of this procedure will be repeated after the test data are analyzed to refine the PID aalgorithm parameters. That would require modifications to sections of the CSTOL script once the new parameters are determined.

5.8 Constraints and Restrictions

Execution of this procedure does not violate any known constraints or restrictions. One operational limitation is noted herein.

6. Operations

6.1 General

6.1.1 This procedure should be performed following the successful execution of an SRE operational

procedure.

6.1.2 This procedure is not to be considered requirements verification. Many of the software algorithms to be used are untested. Where test limits are shown, they are considered a guideline to indicate an expected or typical value. **In case of an out of limits failure, do not stop the testing, but merely note the failure and proceed with the next steps.**

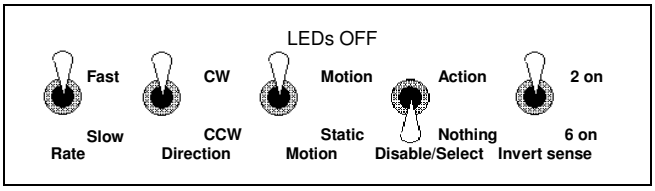
6.1.3 The SRE testset VDC, LMMS #P480213C, contains the version level of all software loaded into the test set. A copy of the current VDC should be attached to this procedure, annotated to indicate any changes that might have occurred to the delivered software. Systems engineering to provide a copy for archive.

QA note _____

6.2 Preliminary Setup

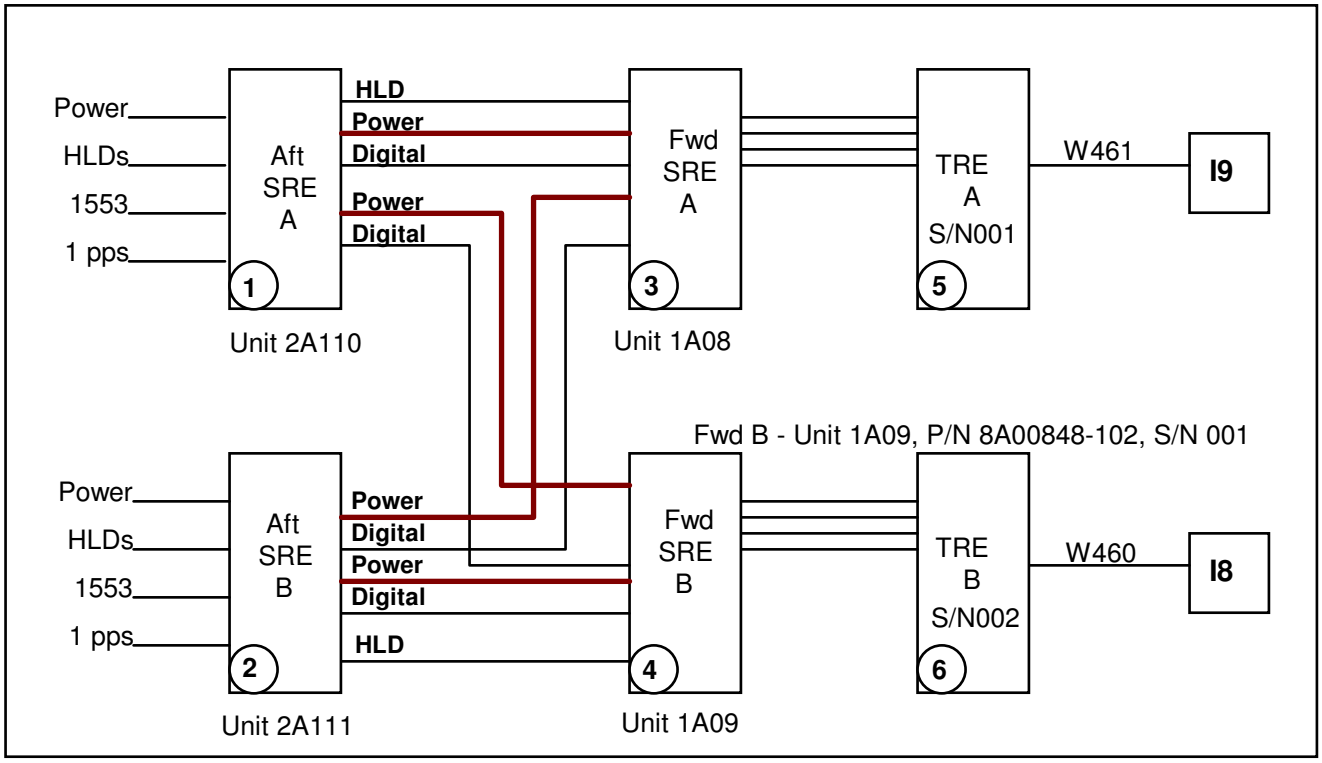
6.2.1 If AS3 is installed on the probe, all of its internal light sources should be powered off for the dark (noise) data collection. Also, **no electrical connections** from AS3 electronics to the SRE, the SRE test set, or the TRE shall be connected during this procedure.

6.2.2 If AS3 is not installed, install the Octolite following the steps in section 12.2 (through 12.2.6) of P0753 Rev. B. Set the Octolite switches so all of the LEDs are off, as shown in paragraph 12.8.1 of P0753 Rev. B.



6.2.3 Be sure to install the aluminum foil to block extraneous light from entering the probe now!

6.2.4 Identify and record the configuration actually installed for this test. The following diagram shows the nominal configuration with all of the hardware available.



6.2.5 Record the identity (Serial Number or Part number) of the boxes in the table below. If a box is not present, indicate "NP"

Circled Number	Unit name	Serial Number or Part Number	Comment
1	Aft SRE		
2	Aft SRE		
3	Forward SRE (A-side)		
4	Forward SRE (B-Side)		
5	A-side TRE	S/N001 Verify	Connects to I9
6	B-side TRE	S/N002 Verify	Connects to I8

6.2.6 If boxes are not present, indicate the connection of the forward SRE to the AFT SRE, regarding the two digital cables terminate.

Fwd Digital	Aft Digital 5 or 6	Comments
Fwd J5	Aft J_____	
Fwd J6	Aft J_____	

6.3 Initial Startup

Some of these beginning steps might have been completed through a previously run procedure.

6.3.1 Turn on the Test Set and load the operating system. Follow the Test Set operators procedure.

6.3.2 Turn on the SRE Power using the SRE Spacecraft Emulator if not aalready on.

6.3.3 Complete the Software initialization. P0833 shall have been completed by this time.

6.3.4 Activate the HLDs to power on the appropriate SRE units and the TRE A and/or TRE B using the display on the SRE Spacecraft Emulator.

6.3.5 Start the CSTOL procedure plv2trei, which will perform many of the following steps.

6.3.5.1 Initialize the Aft SRE

6.3.5.2 Initialize CSTOL monitor displays

6.3.5.3 Initialize Software processes to obtain TRE data.

6.3.5.4 Start Bridge files for tre status

6.4 TRE Operations and data gathering

6.4.1 Power on the TREs (performed by the CSTOL script).

6.4.2 When numbers begin to appear in the monitor displays that look to represent voltages, and the script has advanced to the wait following the label “step2_2:”, pause for recording the following data.

6.4.3 Observe that the voltage monitors are near the nominal values. Record the values of the following monitors in the table. Compare the values with the limits in indicate P or F in the Pass/Fail column to indicate whether the value is within the limits. The appendix at the end of this procedure contains a partial listing of the TRE displays, which might aid in locating the following monitors.

Monitor Name	Lower Limit	Upper Limit	Displayed Value	Pass/Fail
ST_SilicDV_PX_A	10 K	80 K		
ST_SilicDV_PX_B	10 K	80 K		
ST_SilicDV_PY_A	10 K	80 K		
ST_SilicDV_PY_B	10 K	80 K		
ST_M12VSuplPX_A	-12.1 V	-11.7 V		
ST_M12VSuplPX_B	-12.1 V	-11.7 V		
ST_M12VSuplPY_A	-12.1 V	-11.7 V		
ST_M12VSuplPY_B	-12.1 V	-11.7 V		
ST_P12VSuplPX_A	11.7 V	12.1 V		
ST_P12VSuplPX_B	11.7 V	12.1 V		
ST_P12VSuplPY_A	11.7 V	12.1 V		
ST_P12VSuplPY_B	11.7 V	12.1 V		
ST_P5VPwrSpPX_A	4.5 V	5.5 V		
ST_P5VPwrSpPX_B	4.5 V	5.5 V		
ST_P5VPwrSpPY_A	4.5 V	5.5 V		
ST_P5VPwrSpPY_B	4.5 V	5.5 V		

That was fun! Now record some more values and determine if they are within the limits.

Monitor Name	Lower Limit	Upper Limit	Displayed Value	Pass/Fail
ST_RefM10VPX_A	-10.1 V	-9.8 V		
ST_RefM10VPX_B	-10.1 V	-9.8 V		
ST_RefM10VPY_A	-10.1 V	-9.8 V		
ST_RefM10VPY_B	-10.1 V	-9.8 V		
ST_RefM4VPX_A	-4.1 V	-3.85 V		
ST_RefM4VPX_B	-4.1 V	-3.85 V		
ST_RefM4VPY_A	-4.1 V	-3.85 V		
ST_RefM4VPY_B	-4.1 V	-3.85 V		
ST_RefP5VPX_A	4.85 V	5.1 V		
ST_RefP5VPX_B	4.85 V	5.1 V		
ST_RefP5VPY_A	4.85 V	5.1 V		
ST_RefP5VPY_B	4.85 V	5.1 V		
ST_RefPP5VPX_A	0.48 V	0.51 V		
ST_RefPP5VPX_B	0.48 V	0.51 V		
ST_RefPP5VPY_A	0.48 V	0.51 V		
ST_RefPP5VPY_B	0.48 V	0.51 V		
ST_LBoxTempPX_A	20 °C	28 °C		
ST_LBoxTempPX_B	20 °C	28 °C		
ST_LBoxTempPY_A	20 °C	28 °C		
ST_LBoxTempPY_B	20 °C	28 °C		

6.5 Local Closed Loop Heating

6.5.1 Begin heating the detector platforms to 85 K using local closed loop control with update rate set to 7. **Wait until the temperature indication for each platform is higher than 50 K before turning on the detector power.** *This is a documented limitation for the system.*

6.5.2 Continue from the wait following the label “step2_2:”.

6.5.3 The CSTOL will prompt for temperatures for the DMAs. Set the values according to the following table:

DMA indicator	Temp	Value to enter
A-side, X-axis	50K	2194
A-side, Y-axis	55K	2178
B-side, X-axis	60K	2162
B-side, Y-axis	65K	2145

6.5.4 Record the Servo Error Signals in the table below. No Pass/Fail required.

Monitor Name	Displayed Value
ST_TpSvErVtPX_A	
ST_TpSvErVtPX_B	
ST_TpSvErVtPY_A	
ST_TpSvErVtPY_B	

6.5.5 The CSTOL will again prompt for temperature inputs. Set the values according to the following table and then let the procedure continue.

DMA indicator	Temp	Value to enter
A-side, X-axis	70K	2129
A-side, Y-axis	75K	2112
B-side, X-axis	85K	2077
B-side, Y-axis	75K	2112

6.5.6 At the wait following label “step2_3_1:”, verify that the temperatures of the detector platforms are above 50 K. If they are, then type go to continue.

6.5.7 The procedure will turn on the detector power for each detector module.

6.5.8 Wait 5 minutes. the program has a timed wait followed by a hard wait following label “lcldtemp3:”

6.5.9 Record the Servo Error Signals in the table below. No Pass/Fail required.

Monitor Name	Displayed Value
ST_TpSvErVtPX_A	
ST_TpSvErVtPX_B	
ST_TpSvErVtPY_A	
ST_TpSvErVtPY_B	

6.5.10 Continue from the wait following “lcldtemp3:”.

6.5.11 The procedure will again prompt for temperature inputs. Enter the values from the following table.

DMA indicator	Temp	Value to enter
A-side, X-axis	85K	2077
A-side, Y-axis	85K	2077
B-side, X-axis	85K	2077
B-side, Y-axis	85K	2077

6.5.12 The procedure will continue with a timed wait while the temperatures are stabilizing, and then bridge files will be halted.

6.6 Balancing algorithm

6.6.1 Type go following the wait after label “step2_3_2:”. New bridge files will be started.

6.6.2 Type go following label “lcl_dma_bal:”

6.6.3 Run Detector balancing algorithm (Balance mode = 0). When the algorithm completes, record the values for the following monitors in the table as hexadecimal digits. Unless both TREs are active, one set of numbers will likely be at an end point value (0000h).

Monitor Name	Hexadecimal Value
ST_DOffstCmdX_A	
ST_DOffstCmdY_A	
ST_DOffstCmdX_B	
ST_DOffstCmdY_B	

6.6.4 Record the completion status of the algorithm (Offset balancing status) in the table below. Indicate Standby or Done with a check in the appropriate column.

Monitor name	Standby	Done
PT_OfstBlncMX_A		
PT_OfstBlncMX_B		
PT_OfstBlncMY_A		
PT_OfstBlncMY_B		
PT_OfstBlncPX_A		
PT_OfstBlncPX_B		
PT_OfstBlncPY_A		
PT_OfstBlncPY_B		

6.6.5 Set the gain for all detector channels to 8.

6.6.6 Whenever a gain change is made, run a script to update the calibrations based on TRE gain code. (unitswap.prc) Jump to label “step3_1_1:” in plv2trei. (This step could be delayed until after the completion of the clamp adjustment.)

6.6.6.1 At the wait, after unit_swap has completed, go to the appropriate lable to continue.....

6.6.7 Go to label “lcl_clamps:” to run the clamp setting algorithm (Balance mode = 1). When the algorithm completes, record the hexadecimal values for the following monitors in the table below.

Monitor Name	Hexadecimal Value
ST_DClampCmdX_A	
ST_DClampCmdY_A	
ST_DClampCmdX_B	
ST_DClampCmdY_B	

6.6.8 Record the completion status of the algorithm (Clamp balancing status) in the table below. Indicate Standby or Done with a check in the appropriate column.

Monitor name	Standby	Done
PT_ClmpBlncMX_A		
PT_ClmpBlncMX_B		
PT_ClmpBlncMY_A		
PT_ClmpBlncMY_B		
PT_ClmpBlncPX_A		
PT_ClmpBlncPX_B		
PT_ClmpBlncPY_A		
PT_ClmpBlncPY_B		

6.6.9 Continue through the procedure to turn off the detector power and the Local closed loop temperature control. Record the time when temperature control is disabled and the bridge files have been stopped.

Time: _____

6.7 PID temperature control

The PID control will follow a similar temperature profile as that used for the local closed loop control demonstration.

6.7.1 Wait until the indicated temperatures of the detetor platforms fall below 60K before proceeding.

6.7.2 Following label “step3_3:” the CSTOL procedure will initialize the PID algorithm to temperatures as shown in the following table.

DMA indicator	Temp
A-side, X-axis	50K
A-side, Y-axis	55K
B-side, X-axis	60K
B-side, Y-axis	65K

6.7.3 after the temperatures are selected and the PIL control is activated, there is a programmed 10 minute wait, rollowed by automated setting to the following temperatures.

DMA indicator	Temp
A-side, X-axis	70K
A-side, Y-axis	75K
B-side, X-axis	85K
B-side, Y-axis	75K

6.7.4 After the timed five minute wait, record the platform temperatures in the following table.

Monitor	Temperature, K
ST_DiodBiasPX_A	
ST_DiodBiasPX_B	
ST_DiodBiasPY_A	
ST_DiodBiasPY_B	

6.7.5 If all of the temperatures are above 50 K, type go to turn on the detectors. If the temperatures are not near the setpoints of the table in paragraph 6.7.3, it indicates that the PID control algorithm is not functioning properly. This might be an indication to halt the testing and review the bridge files to determine the nature of the PID failure.

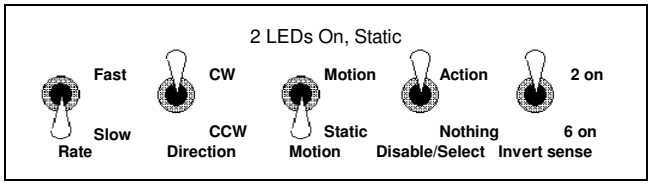
6.7.6 Assuming all is well, continue from the wait following label "lcldet_pwr_on2:" to tuen on the detector power.

6.7.7 A timed wait of five minutes allows the PID to readjust for the added detector dissipation.

6.7.8 The procedure then set the PID Control temperature to 80 K and there is a five minute timed wait.

6.7.9 During the timed wait, illuminate the detectors with the Octolite.

6.7.9.1 Set the switches on the Octolite so two LEDs are illuminated as shown in the figure.



6.7.9.2 The procedure will start several bridge files recording the Science slopes and the detector platform temperatures: (tre_scislp_br, tre_tsrvo_br) and then come to a fixed wait.

6.7.10 Pause at the wait for at least three minutes. Record the time when the wait is terminated.

CSTOL operation resumed at: _____

6.7.11 Type go to restart the operation, The procedure will prompt for gain changes.

6.7.12 Change the gain value to **9** for each detector channel.

6.7.13 After the gain settings are changed the procedure will unit_swap.

6.7.14 Rerun the clamp algorithm if gains are changed and record the new clamp settings in the table below:

Monitor Name	Hexadecimal Value
ST_DClampCmdX_A	
ST_DClampCmdY_A	

ST_DClampCmdX_B	
ST_DClampCmdY_B	

6.7.15 Continue to record datafor several minutes, keeping the illumination constant

6.7.16 Estimate the Heater voltage required to maintain the temperature at 85 K. Record the Heater voltages in the table below:

Monitor Name	Heater voltage
ST_HtrVoltPX_A	
ST_HtrVoltPX_B	
ST_HtrVoltPY_A	
ST_HtrVoltPY_B	

6.7.17 Record the heater command and the value in hexadecimal and decimal in the table below

Monitor name	Hex value	Decimal value
ST_DHeatCmdX_A	H	
ST_DHeatCmdY_A	H	
ST_DHeatCmdX_B	H	
ST_DHeatCmdY_B	H	

6.7.18 The CSTOL should continue to a wait following label “step3_4:” which will have disabled the PID temperature control stopped bridge files and cleared some displays.

6.8 Open loop Temperature stability

6.8.1 Continue by typing go.

6.8.2 Command the Heater voltage to provide the estimated values to maintain 85K using the values recorded above in paragraph 6.7.17.

6.8.3 Go to label “step3_6:”

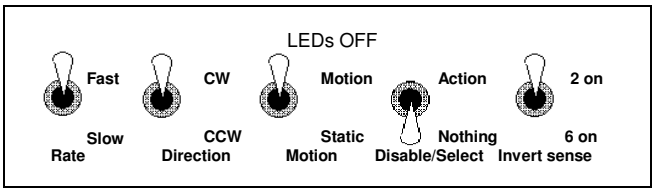
6.8.4 Record data for ten minutes

6.8.5 Record the approximate starting time: _____

6.8.6 When ten minutes have passed, type go to close the bridge files.

6.9 Collect data with the detectors dark.

6.9.1 Set the switches on the Octolite to turn off all of the LEDs as shown in the figure at the right.



6.9.2 Go to label “step3_6:” .

6.9.3 Record data for ten minutes

6.9.4 Record the approximate starting time: _____

6.9.5 When ten minutes have passed, type go to close the bridge files.

6.10 Operation with AS3.

6.10.1 The TREs will not be used to collect AS3 data when used with the SREs under OASIS/CSTOL control.

6.11 Turning off

6.11.1 Go to label “finish:”, and type go to begin an orderly shutdown of the procedure.

6.11.2 Stop recording Bridge Files.

6.11.3 Turn off the Detector power to each module off. (performed by CSTOL script.)

6.11.4 Turn off the TRE power with commands to the SRE (performed by CSTOL script.)

6.11.5 Restore the FAB commands for the TREs.

6.11.6 Turn off the TRE power high level discrete using the SRE Spacecraft Emulator. **Do not turn off the SRE power**.

6.11.7 Archive the data.

Transfer the bridge files to the Payload Server and record the name of the directory in which they are located.

Directory name: _____

QA Witness _____ Date:_____

6.11.8 Notify the data analyst of the availibity and storage location of the the test data.

Peter Boretsky notified: Time and date: _____

7. Test completed.

Completed by: _____

QA Witnessed by: _____

Date: _____

Time: _____

PTD_____ Date _____

Quality
Manager_____ Date _____

8. Appendix--TRE Displays and the Monitors Contained

Display	TRE_AmpV	TRE_ATC_Slope_A	TRE_ATC_Slope_B	TRE_FdBck	TRE_Slope	TRE_StgBias
Mon 1	ST_RsetDrLvPX_A	ST_ATCSlopeMX_A	ST_ATCSlopeMX_B	ST_FdBckPtMX_A	ST_ATCSlopeMX_A	ST_DiodBiasPX_A
Mon 2	ST_RsetDrLvPX_B	ST_ATCSlopeMY_A	ST_ATCSlopeMY_B	ST_FdBckPtMX_B	ST_ATCSlopeMX_B	ST_DiodBiasPX_B
Mon 3	ST_RsetDrLvPY_A	ST_ATCSlopePX_A	ST_ATCSlopePX_B	ST_FdBckPtMY_A	ST_ATCSlopeMY_A	ST_DiodBiasPY_A
Mon 4	ST_RsetDrLvPY_B	ST_ATCSlopePY_A	ST_ATCSlopePY_B	ST_FdBckPtMY_B	ST_ATCSlopeMY_B	ST_DiodBiasPY_B
Mon 5		RT_Mean10HMMX_A	RT_Mean10HMMX_B	ST_FdBckPtPX_A	ST_ATCSlopePX_A	ST_TmpCdDACPX_A
Mon 6		RT_Mean10HMMY_A	RT_Mean10HMMY_B	ST_FdBckPtPX_B	ST_ATCSlopePX_B	ST_TmpCdDACPX_B
Mon 7		RT_Mean10HMPX_A	RT_Mean10HMPX_B	ST_FdBckPtPY_A	ST_ATCSlopePY_A	ST_TmpCdDACPY_A
Mon 8		RT_Mean10HMPY_A	RT_Mean10HMPY_B	ST_FdBckPtPY_B	ST_ATCSlopePY_B	ST_TmpCdDACPY_B
Mon 9		ST_SciSlopeMX_A	PT_Sanity_MX_B	ST_HtrVoltPX_A	ST_SciSlopePX_A	ST_TpSvErVtPX_A
Mon 10		ST_SciSlopeMY_A	PT_Sanity_MY_B	ST_HtrVoltPX_B	ST_SciSlopePX_B	ST_TpSvErVtPX_B
Mon 11		ST_SciSlopePX_A	PT_Sanity_PX_B	ST_HtrVoltPY_A	ST_SciSlopePY_A	ST_TpSvErVtPY_A
Mon 12		ST_SciSlopePY_A	PT_Sanity_PY_B	ST_HtrVoltPY_B	ST_SciSlopePY_B	ST_TpSvErVtPY_B
Mon 13		PT_Sanity_MX_A	ST_SciSlopeMX_B		ST_SciSlopeMX_A	
Mon 14		PT_Sanity_MY_A	ST_SciSlopeMY_B		ST_SciSlopeMX_B	
Mon 15		PT_Sanity_PX_A	ST_SciSlopePX_B		ST_SciSlopeMY_A	
Mon 16		PT_Sanity_PY_A	ST_SciSlopePY_B		ST_SciSlopeMY_B	
Mon 17						
Mon 18						
Mon 19						
Mon 20						

TRE Displays and their Monitors

Display	TRE_MaxMin_Reset	TRE_MnRst_SigCom	TRE_Sci_SlopeInt	TRE_SciSlope_Mkv	TRE_SigCom_Mkv
Mon 1	RT_DetHiValMX_A	RT_Mean10HMMX_A	ST_SciSlopeMX_A	ST_SciMarkMX_A	RT_SigComm0X_A
Mon 2	RT_DetHiValMX_B	RT_Mean10HMMX_B	ST_SciSlopeMX_B	ST_SciMarkMX_B	RT_SigComm0X_B
Mon 3	RT_DetHiValMY_A	RT_Mean10HMMY_A	ST_SciSlopeMY_A	ST_SciMarkMY_A	RT_SigComm0Y_A
Mon 4	RT_DetHiValMY_B	RT_Mean10HMMY_B	ST_SciSlopeMY_B	ST_SciMarkMY_B	RT_SigComm0Y_B
Mon 5	RT_DetHiValPX_A	RT_Mean10HMPX_A	ST_SciSlopePX_A	ST_SciMarkPX_A	RT_SigComm1X_A
Mon 6	RT_DetHiValPX_B	RT_Mean10HMPX_B	ST_SciSlopePX_B	ST_SciMarkPX_B	RT_SigComm1X_B
Mon 7	RT_DetHiValPY_A	RT_Mean10HMPY_A	ST_SciSlopePY_A	ST_SciMarkPY_A	RT_SigComm1Y_A
Mon 8	RT_DetHiValPY_B	RT_Mean10HMPY_B	ST_SciSlopePY_B	ST_SciMarkPY_B	RT_SigComm1Y_B
Mon 9	RT_DetLoValMX_A	RT_SigComm0X_A	ST_SciXceptMX_A		RT_SigComm2X_A
Mon 10	RT_DetLoValMX_B	RT_SigComm0X_B	ST_SciXceptMX_B		RT_SigComm2X_B
Mon 11	RT_DetLoValMY_A	RT_SigComm0Y_A	ST_SciXceptMY_A		RT_SigComm2Y_A
Mon 12	RT_DetLoValMY_B	RT_SigComm0Y_B	ST_SciXceptMY_B		RT_SigComm2Y_B
Mon 13	RT_DetLoValPX_A	RT_SigComm1X_A	ST_SciXceptPX_A		ST_SciMarkMX_A
Mon 14	RT_DetLoValPX_B	RT_SigComm1X_B	ST_SciXceptPX_B		ST_SciMarkMX_B
Mon 15	RT_DetLoValPY_A	RT_SigComm1Y_A	ST_SciXceptPY_A		ST_SciMarkMY_A
Mon 16	RT_DetLoValPY_B	RT_SigComm1Y_B	ST_SciXceptPY_B		ST_SciMarkMY_B
Mon 17		RT_SigComm2X_A			ST_SciMarkPX_A
Mon 18		RT_SigComm2X_B			ST_SciMarkPX_B
Mon 19		RT_SigComm2Y_A			ST_SciMarkPY_A
Mon 20		RT_SigComm2Y_B			ST_SciMarkPY_B

TRE Displays and their Monitors

Display	TRE_House1	TRE_House2	TRE_House3	ECU_I5_TRE	TRE_VoltSanity	TRE_RefVolts
Mon 1	ST_LBoxTempPX_A	ST_TpSvErVtPX_A	ST_RsetDrLvPX_A	PF_Vehicle_Time	PT_Sanity_PX_A	ST_RefPP5VPX_A
Mon 2	ST_LBoxTempPX_B	ST_TpSvErVtPX_B	ST_RsetDrLvPX_B	SF_Format_ID	PT_Sanity_PX_B	ST_RefPP5VPX_B
Mon 3	ST_LBoxTempPY_A	ST_TpSvErVtPY_A	ST_RsetDrLvPY_A	SF_Frame_Count	PT_Sanity_PY_A	ST_RefM10VPX_A
Mon 4	ST_LBoxTempPY_B	ST_TpSvErVtPY_B	ST_RsetDrLvPY_B	TE_TelD_1_GT12Q	PT_Sanity_PY_B	ST_RefM10VPX_B
Mon 5	ST_DiodBiasPX_A	ST_RefM10VPX_A	ST_TmpCdDACPX_A	TE_TelD_2_GT13Q	PT_Sanity_MX_A	ST_RefM4VPX_A
Mon 6	ST_DiodBiasPX_B	ST_RefM10VPX_B	ST_TmpCdDACPX_B	TE_TelCP_1GT14Q	PT_Sanity_MX_B	ST_RefM4VPX_B
Mon 7	ST_DiodBiasPY_A	ST_RefM10VPY_A	ST_TmpCdDACPY_A	DE_Mux1A_CAL2	PT_Sanity_MY_A	ST_RefP5VPX_A
Mon 8	ST_DiodBiasPY_B	ST_RefM10VPY_B	ST_TmpCdDACPY_B	TE_TelCP_2GT15Q	PT_Sanity_MY_B	ST_RefP5VPX_B
Mon 9	ST_FdBckPtMX_A	ST_RefM4VPX_A		DE_Mux1B_CAL2		ST_RefP5VPY_A
Mon 10	ST_FdBckPtMX_B	ST_RefM4VPX_B		TE_SciTel_ST16Q		ST_RefP5VPY_B
Mon 11	ST_FdBckPtMY_A	ST_RefM4VPY_A		DE_Mux7B_SD2_C1		ST_RefPP5VPY_A
Mon 12	ST_FdBckPtMY_B	ST_RefM4VPY_B		TE_Win_4_aPT29P		ST_RefPP5VPY_B
Mon 13	ST_FdBckPtPX_A	ST_RefP5VPX_A		TE_Win_4_bPT30P		ST_RefM10VPY_A
Mon 14	ST_FdBckPtPX_B	ST_RefP5VPX_B				ST_RefM10VPY_B
Mon 15	ST_FdBckPtPY_A	ST_RefP5VPY_A				ST_RefM4VPY_A
Mon 16	ST_FdBckPtPY_B	ST_RefP5VPY_B				ST_RefM4VPY_B
Mon 17	ST_HtrVoltPX_A	ST_RefPP5VPX_A				
Mon 18	ST_HtrVoltPX_B	ST_RefPP5VPX_B				
Mon 19	ST_HtrVoltPY_A	ST_RefPP5VPY_A				
Mon 20	ST_HtrVoltPY_B	ST_RefPP5VPY_B				

TRE Displays and their Monitors

Display	TRE_ATCSlope	TRE_AmalgamPX_A	TRE_AmalgamPX_B	TRE_AmalgamPY_A	TRE_AmalgamPY_B	TRE_DetHiLo
Mon 1	ST_ATCSlopeMX_A	ST_DirClampMX_A	ST_DirClampMX_B	ST_DirClampMY_A	ST_DirClampMY_B	RT_DetHiValMX_A
Mon 2	ST_ATCSlopeMX_B	ST_FdBckPtMX_A	ST_FdBckPtMX_B	ST_FdBckPtMY_A	ST_FdBckPtMY_B	RT_DetHiValMX_B
Mon 3	ST_ATCSlopePX_A	ST_DirClampPX_A	ST_DirClampPX_B	ST_DirClampPY_A	ST_DirClampPY_B	RT_DetHiValPX_A
Mon 4	ST_ATCSlopePX_B	ST_FdBckPtPX_A	ST_FdBckPtPX_B	ST_FdBckPtPY_A	ST_FdBckPtPY_B	RT_DetHiValPX_B
Mon 5	PT_Sanity_MX_A	ST_SciSlopeMX_A	ST_SciSlopeMX_B	ST_SciSlopeMY_A	ST_SciSlopeMY_B	RT_DetLoValMX_A
Mon 6	PT_Sanity_MX_A	ST_HtrVoltPX_A	ST_HtrVoltPX_B	ST_HtrVoltPY_A	ST_HtrVoltPY_B	RT_DetLoValMX_B
Mon 7	PT_Sanity_MX_A	ST_SciSlopePX_A	ST_SciSlopePX_B	ST_SciSlopePY_A	ST_SciSlopePY_B	RT_DetLoValPX_A
Mon 8	PT_Sanity_MX_A	ST_TpSvErVtPX_A	ST_TpSvErVtPX_B	ST_TpSvErVtPY_A	ST_TpSvErVtPY_B	RT_DetLoValPX_B
Mon 9	PT_Sanity_MX_A	ST_TmpCdDACPX_A	ST_TmpCdDACPX_B	ST_TmpCdDACPY_A	ST_TmpCdDACPY_B	RT_DetLoValPY_A
Mon 10	PT_Sanity_MX_A	ST_LBoxTempPX_A	ST_LBoxTempPX_B	ST_LBoxTempPY_A	ST_LBoxTempPY_B	RT_DetLoValPY_B
Mon 11	ST_ATCSlopeMY_A					RT_DetHiValMY_A
Mon 12	ST_ATCSlopeMY_B					RT_DetHiValMY_B
Mon 13	ST_ATCSlopePY_A					RT_DetHiValPY_A
Mon 14	ST_ATCSlopePY_B					RT_DetHiValPY_B
Mon 15						RT_DetLoValMY_A
Mon 16						RT_DetLoValMY_B
Mon 17						
Mon 18						
Mon 19						
Mon 20						

TRE Displays and their Monitors

Display	TRE_MeanandSig	TRE_SigOffRset	TRE_MarkandSlope	TRE_XceptTpTmp
Mon 1	RT_Mean10HMMX_A	RT_SigComm2X_A	ST_SciMarkMX_A	ST_SciXceptMX_A
Mon 2	RT_Mean10HMMX_B	RT_SigComm2X_B	ST_SciMarkMX_B	ST_SciXceptMX_B
Mon 3	RT_Mean10HMPX_A	RT_SigComm2Y_A	ST_SciMarkPX_A	ST_SciXceptPX_A
Mon 4	RT_Mean10HMPX_B	RT_SigComm2Y_B	ST_SciMarkPX_B	ST_SciXceptPX_B
Mon 5	RT_SigComm0X_A	ST_RsetDrLvPY_A	ST_SciSlopeMX_A	ST_TmpCdDACPX_A
Mon 6	RT_SigComm0X_B	ST_RsetDrLvPY_B	ST_SciSlopeMX_B	ST_TmpCdDACPX_B
Mon 7	RT_SigComm1X_A	ST_RsetDrLvPX_A	ST_SciSlopePX_A	ST_TpSvErVtPX_A
Mon 8	RT_SigComm1X_B	ST_RsetDrLvPX_B	ST_SciSlopePX_B	ST_TpSvErVtPX_B
Mon 9	RT_SigComm1Y_B		ST_SciSlopePY_A	ST_TpSvErVtPY_A
Mon 10	RT_SigComm1Y_B		ST_SciSlopePY_B	ST_TpSvErVtPY_B
Mon 11	RT_Mean10HMMY_A		ST_SciMarkMY_A	ST_SciXceptMY_A
Mon 12	RT_Mean10HMMY_B		ST_SciMarkMY_B	ST_SciXceptMY_B
Mon 13	RT_Mean10HMPY_A		ST_SciMarkPY_A	ST_SciXceptPY_A
Mon 14	RT_Mean10HMPY_B		ST_SciMarkPY_B	ST_SciXceptPY_B
Mon 15	RT_SigComm0Y_A		ST_SciSlopeMY_A	ST_TmpCdDACPY_A
Mon 16	RT_SigComm0Y_B		ST_SciSlopeMY_B	ST_TmpCdDACPY_B
Mon 17				
Mon 18				
Mon 19				
Mon 20				