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Gravity Probe B Relativity Mission

GSS Requirements Verification Analysis Report 1

S0451 Rev. A

7 January 2003

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ITAR Control Required? ☐Yes ☐No

Change Log:

Rev N/C to Rev A, 7 January 2003: MSFC requests for T003 #16.3.2 verification support

1) *Update S0451 to include conditions under which the CPU can be commanded to 'unlock' from the 16fo clock. Provide CARD (or equivalent) that prohibits this command during the mission and/or provide 199A-964-1 and SHS210025.*

   Clarified description of clock switching conditions for the payload processor in "GSS ASU CPU Timing Signal, item 2".

2) *Update S0451 regarding the analysis of the GSS ASU APU Timing Signal and the GSS ASU AMT Timing Signal*.

   Attached two page block diagram of aft and forward GSS boxes that show the generation and routing of the GSS clocks.

Purpose:

The analyses in this document verify two Gyroscope Suspension System (GSS) requirements. The two requirements are defined in PLSE-13, part 1, Revision B, "Gyroscope Suspension System (GSS) Specification and listed in Table 1."

Table 1

PLSE-13 Requirements verified in this document

VRCM Item	Title	Requirement	Method
3.2.8.6.1	16fo clock synchronization	The GSS shall derive all of its timing signals by counting down the SRE 16fo signal, when available, from the aft SRE	A
3.2.8.7	GSS secondary payload clocks	GSS internal timing sources shall be counted from the 16fo clock except the GSS C side (aft) power supply.	A

Acronym List

ACL – Aft Communication Link
ACS – Aft Clock Support
ACU – Aft Control Unit
ADDA – Analog to Digital & Digital to Analog
AMT – Aft Monitor/Timing
APU – Aft Power Unit
ASU – Aft Suspension Unit
CPU – Central Processing Unit
ECU – Experiment Control Unit
EM – Engineering Memo
FMECA – Failure Modes, Effects and Causes Analysis
FPGA – Field Programmable Gate Arrays
FSU – Forward Suspension Unit
GSS – Gyroscope Suspension System
MUX – Multiplexer
PLL – Phase Locked Loop
SRE – Squid Readout Electronics

GSS 3.2.8.6.1 (T003 16.3.2) - 16fo clock synchronization

The GSS shall derive all of its timing signals by counting down the SRE 16fo signal, when available, from the aft SRE.

GSS 3.2.8.7 (T003 16.3.2) - GSS secondary payload clocks

GSS internal timing sources shall be counted from the 16fo clock except the GSS C side (aft) power supply.

The analysis in this document verifies both requirements. The above requirements can be combined to state: "All GSS internal timing signals, except one timing signal for the GSS C side (aft) power supply, shall be synchronized to the SRE 16fo signal when it is available during mission operations."

The intent of this requirement is to ensure phase synchronization with the SRE 16fo reference source. The requirements are interpreted to not exclude the use of amplifier or Phase Locked Loop (PLL) circuits, neither of which affects phase synchronization.

Reference: As-built schematics for GSS FSU 26226-101 and GSS ASU 26225-101. See attached sheets for internal diagrams of the forward and aft GSS units that depict the generation of the internal timing signals in the GSS system.

In requirement 3.2.8.7, the "internal timing sources" are defined to be the GSS secondary payload clocks.

There are a total of five local oscillators in the GSS that act as timing signal sources for the various GSS subsystems. All of these local oscillators are contained in GSS ASU modules ACS, CPU, and APU, and in GSS FSU MUX module. Additional GSS internal timing signals are generated in the GSS ASU AMT module. These additional timing signals are derived from the ACS module, which is referenced to the 16 fo signal, as described below.

1) GSS ASU ACS Timing Signal
   The ASU contains an ACS module (8A01898-101) with an on-board phase-locked loop oscillator circuit. If a 16fo signal from the SRE is present, the PLL will lock to it. If signals from both the 'A' and 'B' sides are present, the 16fo signal on the 'A' side will drive the PLL, and the 'B' side signal will be ignored. The resulting PLL output supplies the highest-frequency reference. This reference clocks all other timing circuits in the ASU and FSU - except for the APU C side aft power supply, which contains an unlocked oscillator at 136,400 Hz and which is specifically exempt from this requirement as stated in GSS 3.2.8.7 above. (Refer to the as-built schematics referenced above)

2) GSS ASU CPU Timing Signal
   The ASU contains a CPU module (199A-964-1) with an on-board oscillator circuit. The module can get its timing signal from either of 2 sources:

   1. The CPU modules own on-board oscillator circuit (not derived from the 16fo signal) or

   2. The 16fo signal from the SRE (via the phase locked loop oscillator on the GSS aft clock support card – ACS)

Code satisfying GSW requirement SHG210091 (*The scheduler shall check the presence of external clock and configure the processor to use the external clock if it is available.*) commands the payload processor to switch to the external SRE 16fo signal. By design, the payload processor cannot be switched back to the on-board clock by software command; it can only be switched by command from internal clock to the external clock. This is performed by the GSW software on initial bootup per SHG21009. Resetting or power cycling the processor, or loss of the external clock, will cause the processor card to revert to its internal clock.

An internal/external clock source status bit is available in telemetry to indicate the synchronization state of the processor.

3) GSS FSU MUX Timing Signal
The FSU contains a MUX module (8A01883-101) with an on-board phase-locked loop oscillator circuit. When a 34,100 Hz signal is received from the FSU FCL module (8A01891-101), the MUX PLL locks onto it. The FCL module's 34,100 Hz signal is derived from the 68,200 Hz signal received from the ACL module (8A01897-101) in the ASU via the GFAB bus. That signal is divided on the ACL from the ACS 16fo reference, which is locked to the SRE 16fo signal. (Refer to the as-built schematics referenced above)

4) GSS ASU APU Timing Signal
The ASU contains an APU module (BE02598075), which has two phase-locked loop oscillator circuits; one at 136,400 Hz and one at 545,600 Hz. (The 545,600 Hz oscillator, for the GSS C side (aft) power supply, is not derived from the SRE 16fo signal and is exempt from this requirement as previously stated). The 545,600 Hz PLL oscillator reference signal is received from the AMT module (8A01899-101), also located in the ASU. The AMT 136,400 Hz signal is divided down, in the AMT Field Programmatic Gate Array (FPGA) (26220) from the ACS module's reference 16fo signal. The ACS module's reference signal is locked to the SRE 16fo signal. (Refer to the as-built schematics referenced above)

5) GSS ASU AMT Timing Signal
The AMT FPGA counts down the ACS SRE-locked 16fo signal to generate two timing strobes at each GSS Mission Mode control rate (220 Hz, 660 Hz, or 1320 Hz) when the strobes are enabled. When enabled, the strobes trigger A/D and D/A converters in the FSU ADDA module (8A01886-101). After leaving the AMT module, the strobe signals are routed by the ABP module (8A01901-101), driven to the GFAB by the ACL, received from the GFAB by the FCL, and routed by the FBP (8A01893-101) to the ADDA module. None of these operations affects timing and the strobe signals remain locked to the SRE 16fo signal. (Refer to the as-built schematics referenced above)

In summary: Three local oscillators (Aft ACS, Fwd MUX and one of the APU oscillators) are always synchronized to the SRE 16fo signal via phase-locked loop circuits. Of the remaining two, the R6000 payload processor initially references it's own on-board oscillator, but only during GSS initialization procedures. Post initialization, the CPU timing reference is switched, by flight software command, to the 16fo signal. The CPU remains locked to that signal for the duration of the mission when the signal is available. The fifth oscillator is in the GSS C side (aft) power supply, which is allowed by GSS 3.2.8.7 not to be locked to the SRE reference.

Therefore, all timing signals are locked to the SRE reference, when available, except the GSS C side (aft) power supply local oscillator and the above requirements are met with respect to the GSS subsystem.

REVISED	PAGE	FILENAME
5/34/02	1 OF 2	S0451A CLOCK DIAGRAM.VSD

Forward Comm Link (FCL)

DA converters (6)

5 kHz Low pass filter

DA trigger

Trigger detect monitor

AD trigger

AD converters (3)

Variable Low Pass Filters (3)

Mode	Filter:
SM:	110 Hz
SU:	220 Hz
GT	660 Hz
PON:	660 Hz

AD trigger

AD converter (1)

Variable Low Pass Filter

ADDA

M Voltages

6

Spinup Position MR[13-11]

3 Spinup Backup (SUB) A

3 Science High Backup (SMHB) B

3 Science Low Backup (SMLB) C

ABU

Voltages

M

6 D E F 6

MUX

Output	Arbiter States:
D:	Prime (1)
E:	All others (2 - 9)
F:	PON (0)

Output	Mode	Arbiter States:
A:	SU, GT	Any
B:	SM	Prime (1), PON (0), HBT (5), HB1 (6), HB2 (7)
C:	SM	LB1 (8), LB2 (9)

MUX

48:1 Mon mux

48 Monitor inputs

68.2 kHz sync for 3 phase oscillator

MUX select word

Arbiter Status Word

Power-on Reset pulse (From ARB)

Mode Register Word (MR[15-0])

Heartbeat detector

Mode	H'Beat:
SM:	220 Hz
SU:	660 Hz
GT	1320 Hz
PON:	Disabled

FMR

Low Postion Threshold

High Postion Threshold

Arbiter State Machine

(Version 7.2 A)

MR bits noted with an asterick are used by the arbiter

Arbiter

Control lines to ABU, MUX, LVA (See selection logic notes, above)

Power-on Reset pulse

Digital 34.1 kHz clock

High Voltage Power (HLD controlled via APU)

Bandwidth = 3 kHz

200

Voltages (x/200)

M

HVA/Brg

6

HV_AMP_SEL MR[6] latch position

Bandwidth = 100 Hz

Prime (bandpass) path

Backup (Lowpass) path

G H

5

Voltages (x/5)

M

LVA

6

LV_AMP_SEL MR[5] latch position

Output	MR[8]	Arbiter States:
G:	0	Prime (1)
H:	1	Prime (1)
H:	X	All other states

Temps

M

3

Position Bridges (3)

6

3

Oscillator Level (Hi/Lo) MR[4]

Analog 34.1 kHz 3 phase clocks

HVA/Brg

68.2 kHz sync for 3 phase oscillator (from FCL)

PLL and 3 phase oscillator

M

PLL effort

Voltages

M

Various scalings

Fwd Voltage Regulator (FRM)

FSU system power

6

To gyroscope electrodes (J41-J46)

M

Charge control bias generateor

To gyroscope charge control electrodes (J48)

Charge control bias command +3/-3/0 V MR[15-14]

To gyroscope groundplane (J47)

Bit numbers are hardware bus bit numbers; software bits are in reverse order

Mode Register Bit Definitons

HW Bit	Function
0*	COMP_OK
1*	LOW_THRESHOLD_ENABLE
2*	MODE0
3*	MODE1
4	OSC_AMP (0=High)
5	HVA_AMP_SELECT (pulse hi)
6	LVA_AMP_SELECT (pulse hi)
7	PON_RST_N (must be cleared in SW)
8*	LVA_P_BU_SEL (0=AOD prime path)
9*	HI_THRESHOLD_ENABLE
10	MR_BIT_10 (unused)
11	SU_R_CMD_1
12	SU_R_CMD_2
13	SU_R_CMD_3
14	M3V_CHRG_ENABLE
15	P3V_CHRG_ENABLE

Arbiter Status Word Bit Definitons

HW Bit	Function
0	Arbiter state 0
1	Arbiter state 1
2	Arbiter state 2
3	Arbiter state 3
4	High backup threshold (1=exceeded)
5	Low backup threshold (1=exceeded)
6	Spinup backup threshold (unused)
7	Max velocity threshold (unused)
8	unused
9	unused
10	unused
11	Mode register busy (active low)
12	unused
13	MR voting error (active high)
14	unused
15	Watchdog error (active high)

GSS FSU Block Diagram

M *MUX monitor points*

REVISED	PAGE	FILENAME
1/7/2003	2 OF 2	S0451A CLOCK DIAGRAM.VSD

Various monitor points

16:1 MUX

AD converter

Bus

1555 A (J3)

1553 B (J4)

J5

1553 programing plut (external)

Test Port (J51)

Aft Test Card (ATC)

M *Temp*

Bus

RAD6000 Processor Card

Bus

Control Logic (FPGA)

From SRE (J6)

10 Hz B

10 Hz A

16fo B

16fo A

16fo A detected

16fo B detected

Opto-isolator receivers and buffers

PRIMARY CLOCK SOURCE FOR GSS STRING (FWD + AFT)

SRE Clocks enable

Dual 2:1 MUX

PLL control effort

M

16fo

10 Hz

Invert 16fo

16fo Oscillator and PLL

Local 16fo

Int0 signal shaper

Int0

APU Clocks Enable

APU Clock Generator

136.4kHz

545.6kHz

ACS

To APU (J12)

Note:
545.6kHz sync not used APU (C side, aft GSS suppy)

Boost computer port (J53)

Aft Comm Link (ACL)

Bus

Bus

To FSU via GFAB Cable (J22, J23)

AD Trigger

DA Trigger

68.2 kHz sync

ACL reset

1.09 Mhz internal clock

Local clock generator

R6000 clock mux:
Local on power up/reset
External on SW command
(cannot be commanded back to internal via SW)

Internal circuitry

2:1 Mux

Local 16fo xtal

Int1 (220/660 Hz)

Int2 (220/660 Hz)

Int3 (220/660 Hz)

16fo Local

Int0 (10Hz)

Clock Generator (FPGA)

AMT

AD trigger

DA trigger

16fo Local

AMT Analog Monitors

Chan	Function
0	External input
1	unused
2	APU temp
3	unused
4	+15 v monitor
5	-15 v monitor
6	+5 v monitor
7	+3.3 V monitor

AMT Analog Monitors

Chan	Function
8	APU HV A power monitor
9	APU HV B power monitor
10	AMT Temperature
11	ATC Temperature
12	ACS PLL control Effort
13	Total 5V current
14	R6000 5V current
15	Digital ground

GSS Aft Control Unit (ACU) Block Diagram